10G BASE-T System Overview

Member : Chien, Ying-Ren
Lee, Jan-Hwa
Advisor : Tsao, Hen-Wai
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Outline

- Introduction
  - 10G connectivity options
  - System overview
  - System requirement
- Channel Models
- Coding & Modulation
- Equalization
- Timing recovery
- Transmitter front end solutions
- Start-up protocol
- References

10G Connectivity Options

Standard	Technology	Media	Reach
10GBASE-SR	850nm 10.3G Serial	62.5µm MMF 50µm MMF	2-33m 2-300m
10GBASE-LX4	1300nm CWDM 4 X 3.125Gbps	50/62.5µm MMF 10µm SMF	2-300m 2-10km
10GBASE-LRM	850 & 1300nm 10.3G Serial EDC	50/62.5µm MMF	.5-300m
10GBASE-CX4	4 X 3.125Gbps	8 Pair Shielded Cu “InfiniBand Cable”	≤15m
10GBASE-T	128DSQ w/FEC @ 800 MHz	Cat 6 Cat 7	55-100m 100m

10GBASE-T：When？

- 2002,Nov : Project Initiation
- 2003,Nov : Project Authorization
- 2004,July : Draft 1
- 2005,Mar : Working Group Ballot
- **2005,July : Draft 2**
- 2006,Jan : Draft 3
- **2006,July : RevCom Standard Released**

IEEE 802.3an : 13 Objectives(1/2)

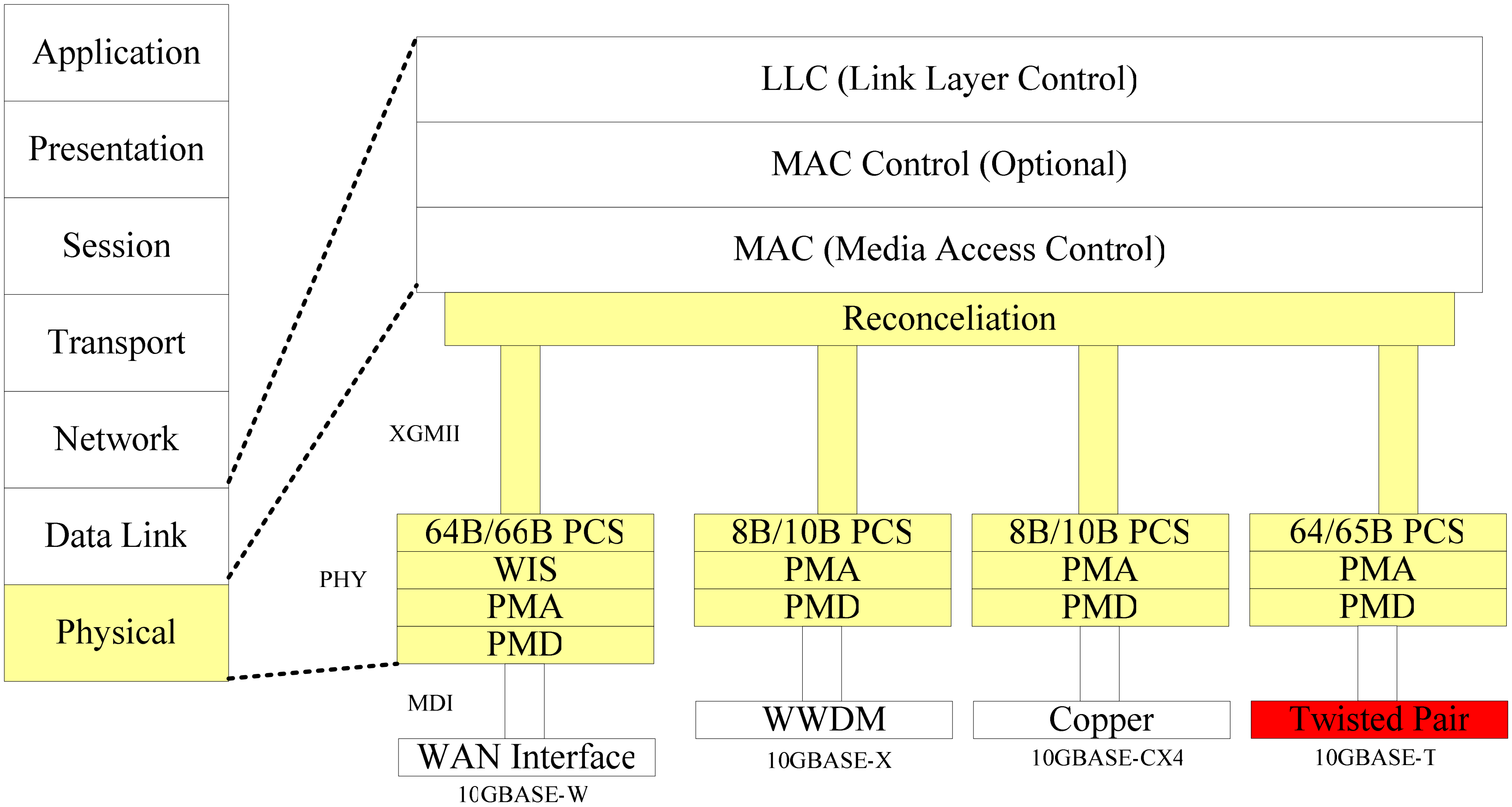
- Preserve Ethernet format size
- Preserve Ethernet frame size
- Support full duplex operation only (No CSMA / CD)
- Will not support 802.3ah (EFM)
  - unidirectional operation EFM is half duplex
- Support a speed of 10Gbps
- Select copper media from ISO/IEC 11801:2002
- Support auto-negotiation
- Support coexistence with 802.3af
- Meet CISPR/FCC Class A

IEEE 802.3an : 13 Objectives(2/2)

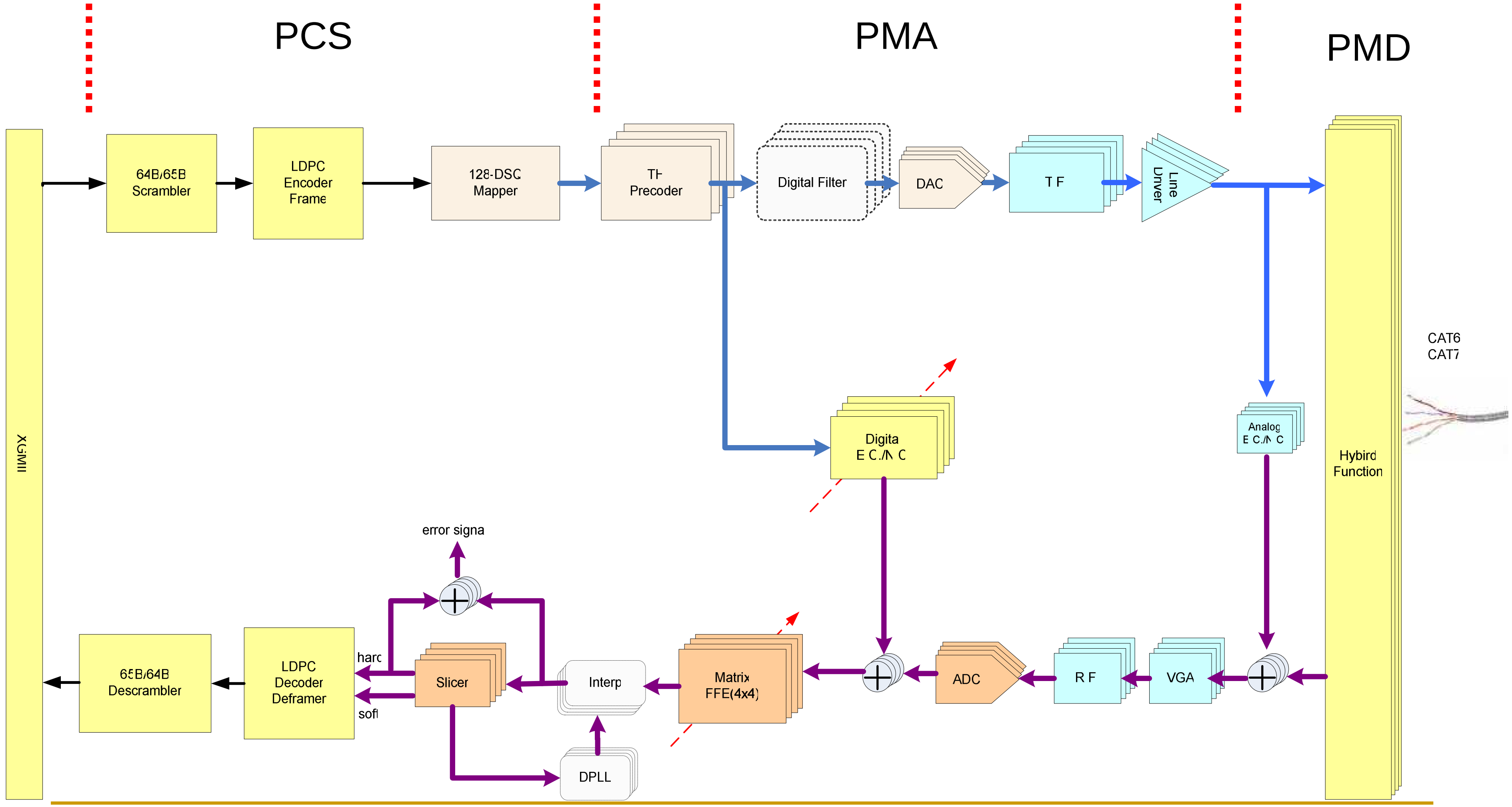
- Support star-wired LANs using structured cabling
- Support operation over 4-connector structured 4-pair,twisted-pair copper cabling
- Define a single 10 Gb/sPHY support links of:
  - 100 m, four-pair Class F(CAT7)
  - 55 m to 100 m, four-pair Class E (CAT 6)
  - 55m CAT 6 unshielded & 100m CAT 6 shielded
- Support a BER of **10^-12** on all supported distances and classes

System Overview

10G Ethernet v.s. OSI Ref Model



10GBASE-T System Block Diagram

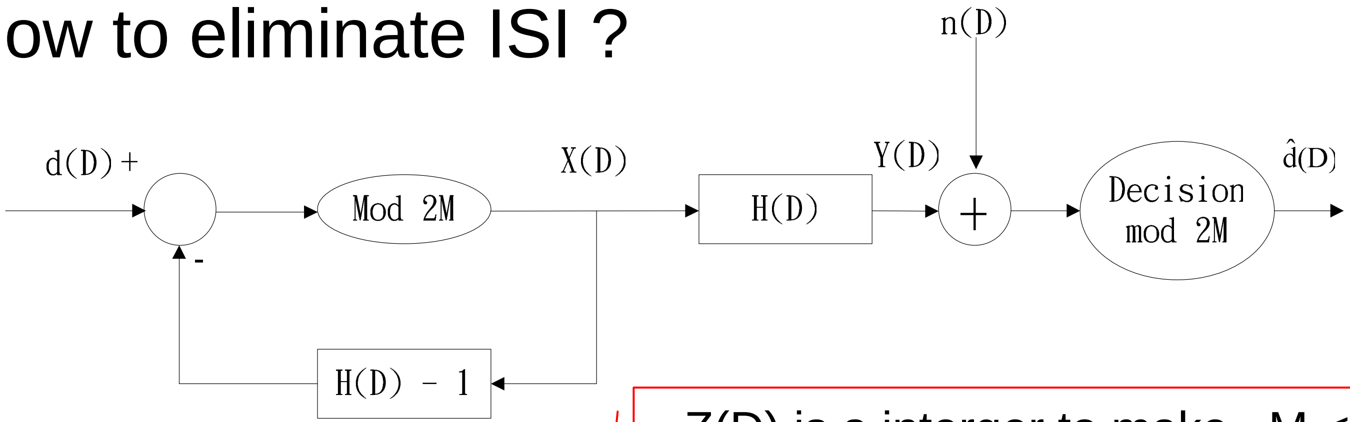


Major TX Path Blocks

- PCS
  - XGMII to 64B/65B scrambler to FEC (LDPC) which is mapped to 128DSQ which is then mapped to 4 channels
- Modulation
  - 16 Level Pulse Amplitude Modulation (16 PAM)
- Tomlinson-Harashima Precoding (THP)
  - Transmit equalization
  - Pre-compensates the signal based on knowledge of the channel
  - Suit for (quasi-)static channel

Introduction of TH Precoding(1/3)

- How to eliminate ISI ?



Z(D) is a interger to make –M < X(D) <M

- Z transform

$$X(D) = d(D) + 2MZ(D) - X(D)[H(D) - 1]$$

- Simplify ➔

$$X(D) = {[d(D) + 2MZ(D)]}\Big/{H(D)} = {Y(D)}\Big/{H(D)}$$

Introduction of TH Precoding(2/3)

- Receiver signal is

$$
\begin{aligned}
r(D) &= X(D)H(D) + n(D) \\
&= Y(D) + n(D) \\
&= d(D) + 2MZ(D) + n(D)
\end{aligned}
$$

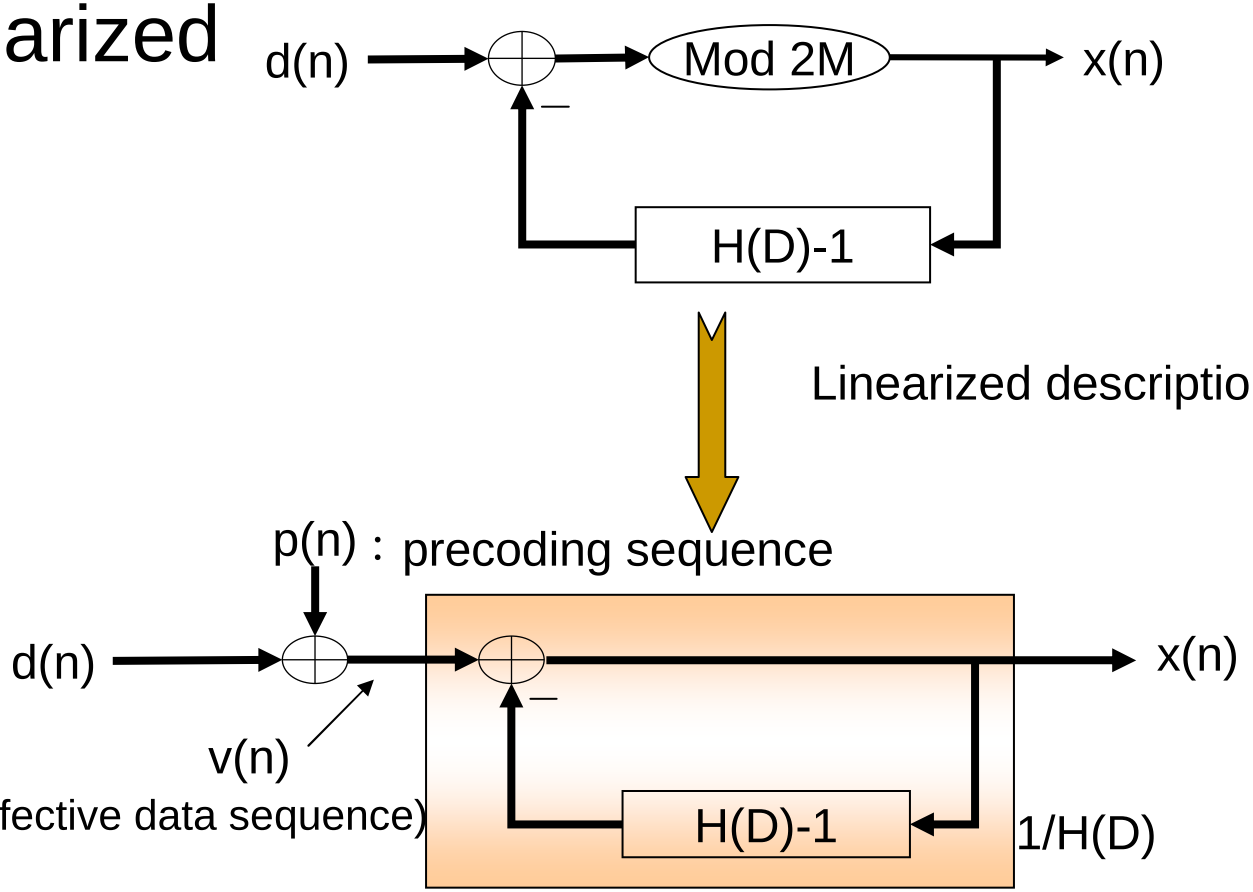
so ISI be eliminated

- After modulo-2M, then

$$\frown{d}(D) = d(D) + n(D)$$

Introduction of TH Precoding(3/3)

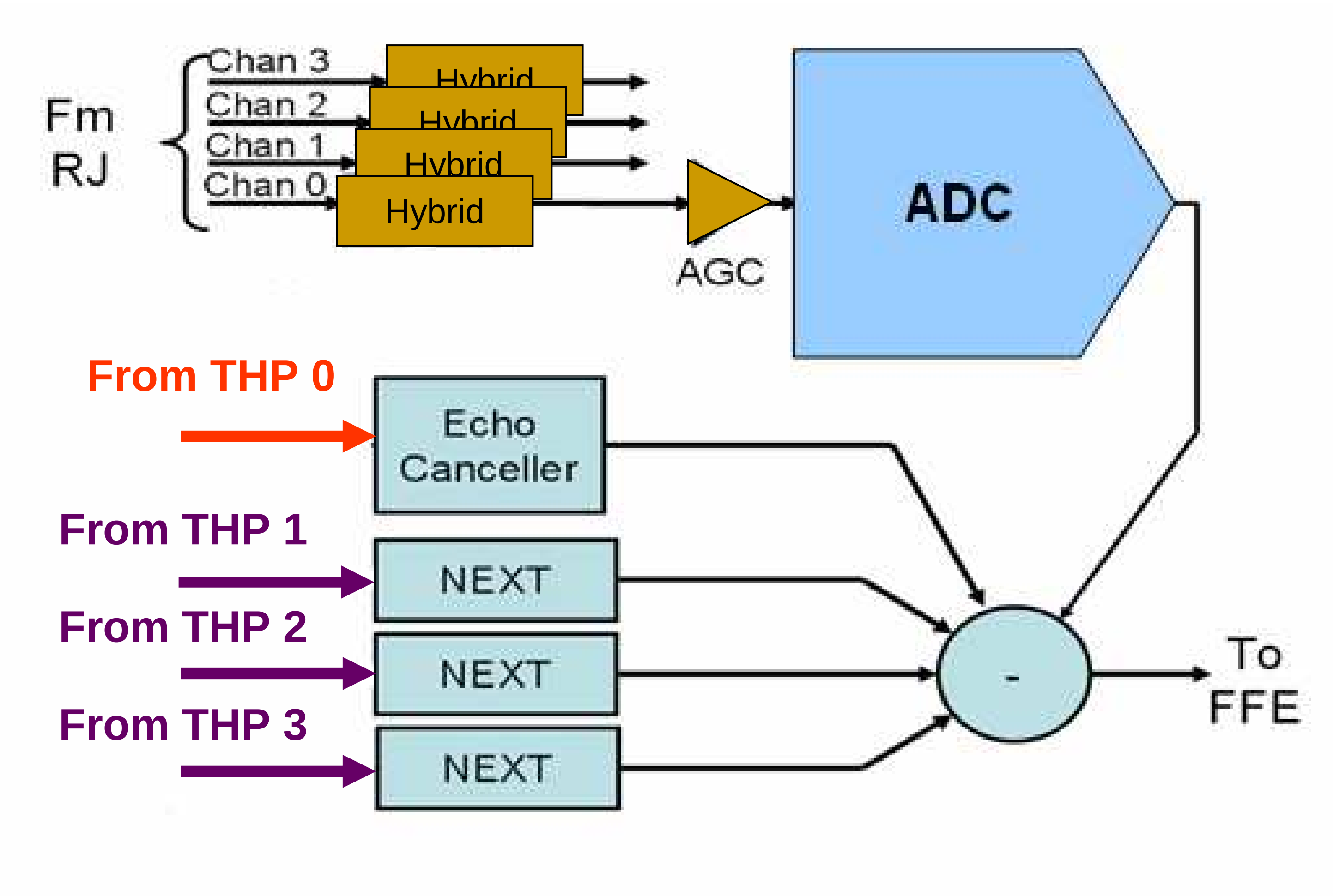
- Linearized



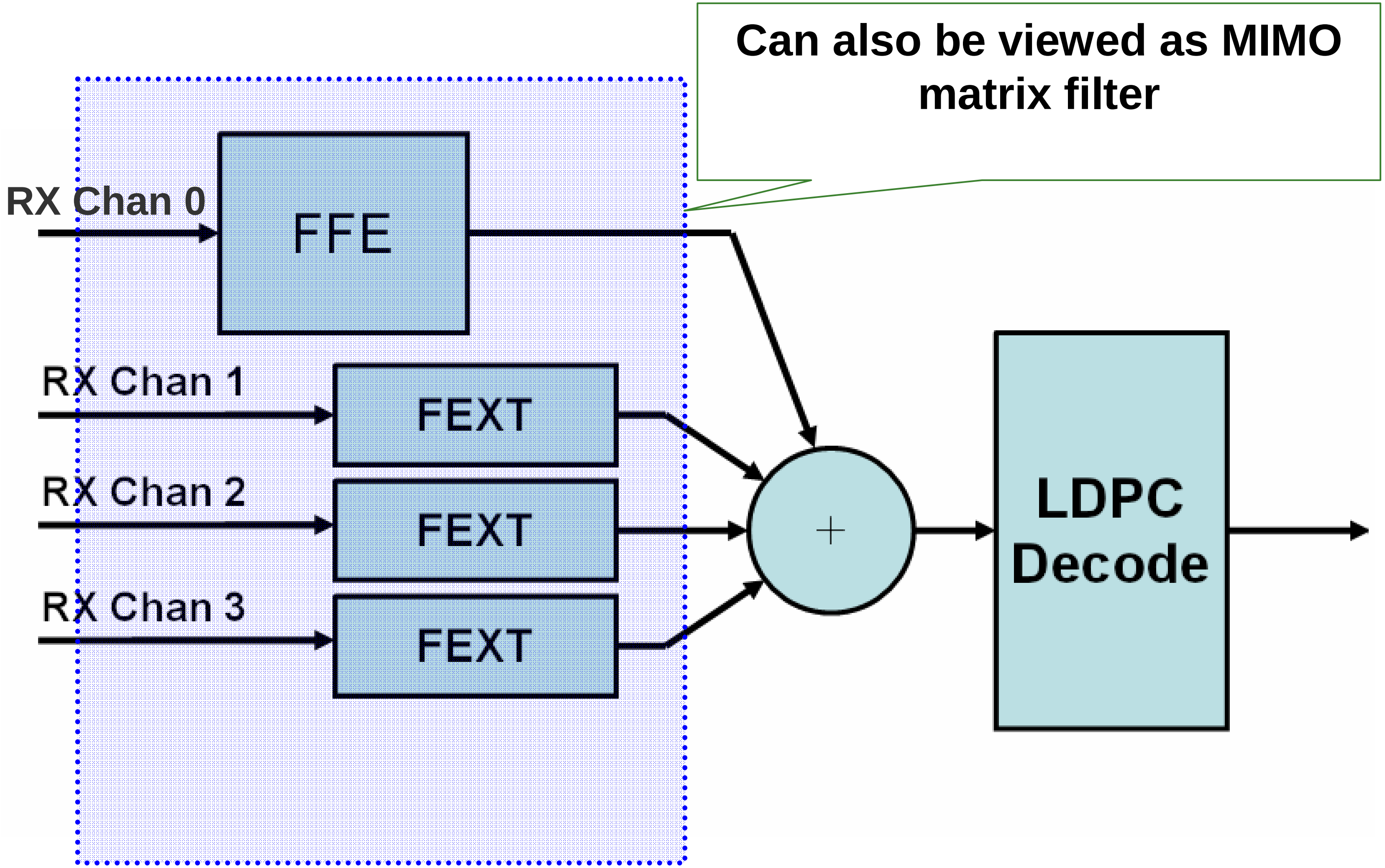
Major RX Path Blocks

- Hybrid function
  - Enable bidirectional data transmission on a single pair
  - Stop the local transmitted signals from being mixed with the local received signals.
- A/D
  - 800MHz, ~ 10bit accuracy
- Echo/NEXT Canceller
- Matrix FFE
- LDPC Decoder
- 65B/64B Descrambler

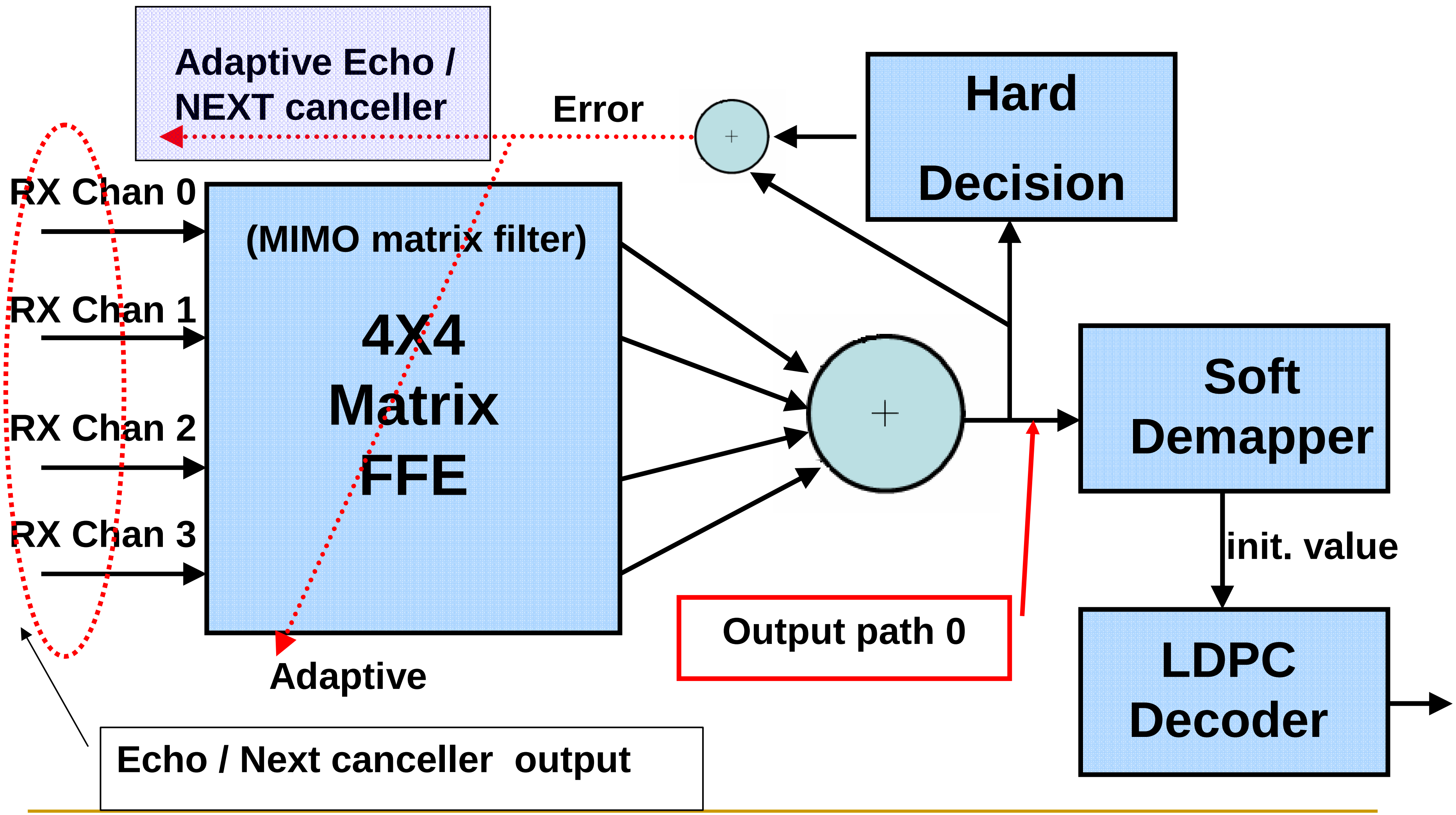
Receiver Path for Channel 0 (1/3)



Receiver Path for Channel 0 (2/3)



Receiver Path for Channel 0 (3/3)



System Requirements

Tentative 10GBASE-T Spec

Modulation Code	Baseband 128-DSQ (PAM-16)
Baud Rate	~ 800 MHz
FEC	LDPC(2048,1723) systematic
Framing	64B/65B
Transmitter Equalization	Tomlinson-Harashima Precoding
Required SNR	23.4dB
Transmit Filter	Spectral mask
Transmit Power	3.2dbm-5.2dbm (center at 4.2dbm) at MDI (Medium dependent interface)
Transmit Voltage	2V +/- 5% at MDI
Receiver Filter	Low order CT
Receiver Equalization	Adaptive FFE
MAC Interface	XGMII

Tentative System Requirements

- assume 15dB analog echo suppression

Echo Suppression	~55dB
NEXT Suppression	~40dB
FEXT Suppression	~25dB
ADC/DAC resolution	10bit
Precoding function	ARMA(3,3) 3 zeros, 3 poles
FFE span	64 taps

Channel Models

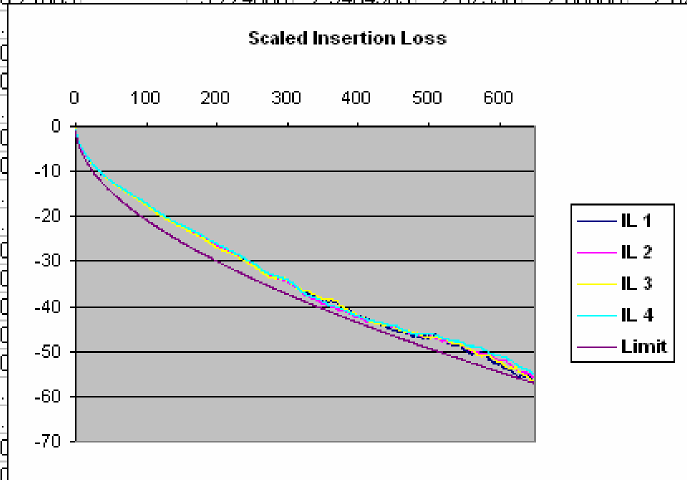
Channel Impairments

- Insertion Loss (I.L.)
- Near End Crosstalk (NEXT)
- Far End Crosstalk (FEXT)
- Echo
- Alien Crosstalk

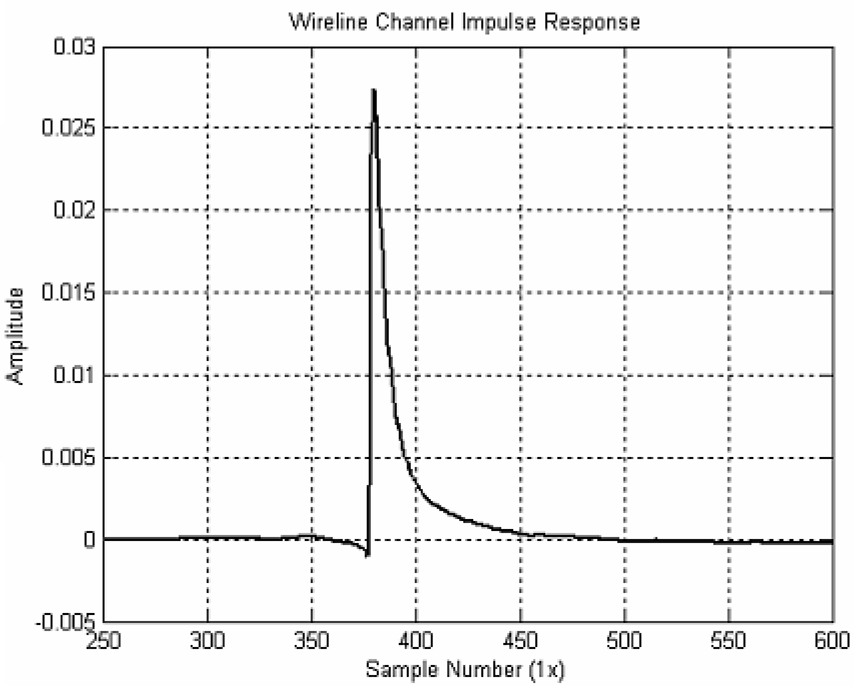
Channel Model Data

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1	Freq	IL 1		IL 2		IL 3		IL 4		Magnitude	Freq	IL 1	IL 2	IL 3	IL 4
2	0.1	0.863964	-0.30576	0.874773	-0.32493	0.893336	-0.32124	0.873472	-0.3213		0.1	-0.7576027	-0.60079	-0.45158	-0.6239
3	0.724938	-0.52166	-0.66651	-0.59449	-0.61808	-0.54812	-0.67975	-0.57884	-0.62907		0.724938	-1.4486412	-1.33452	-1.17763	-1.36207
4	1.349875	-0.50117	0.620482	-0.38227	0.712151	-0.50141	0.651403	-0.41065	0.695254		1.349875	-1.9642919	-1.84896	-1.70221	-1.85746
5	1.974813	0.680175	0.343933	0.758483	0.148257	0.712521	0.33044	0.746677	0.192506		1.974813	-2.3587799	-2.23825	-2.09802	-2.25785
6	2.59975	0.185177	-0.71065	-0.07884	-0.73989	0.158216	-0.73852	-0.02099	-0.74314		2.59975	-2.6815275	-2.56763	-2.43792	-2.5751
7	3.224688	-0.71193	-0.03541	-0.66608	0.279448	-0.73376	0.003108	-0.68898	0.21603		3.224688	-2.9404985	-2.82536	-2.68886	-2.82856
8	3.849625	0.108378	0.666425	0.43778	0.52378	0.154682	0.676186	0.375441	0.		[illegible]	[illegible]	[illegible]	[illegible]	…2478
9	4.474563	0.615006	-0.22779	0.37087	-0.54953	0.613704	-0.28114	0.440375	-0		[illegible]	[illegible]	[illegible]	[illegible]	…5537
10	5.0995	-0.3342	-0.54383	-0.61395	-0.19731	-0.38948	-0.52757	-0.57848	-0		[illegible]	[illegible]	[illegible]	[illegible]	…3011
11	5.724438	-0.45744	0.422203	-0.01902	0.629195	-0.42658	0.476455	-0.12404	0.		[illegible]	[illegible]	[illegible]	[illegible]	…0008
12	6.349375	0.492122	0.359374	0.596838	-0.1528	0.541115	0.314337	0.615765	-0		[illegible]	[illegible]	[illegible]	[illegible]	…9248
13	6.974313	0.253532	-0.53842	-0.30336	-0.51975	0.194767	-0.57768	-0.19289	-0		[illegible]	[illegible]	[illegible]	[illegible]	…9082
14	7.59925	-0.56334	-0.14498	-0.4078	0.424022	-0.59267	-0.07456	-0.49185	0.		[illegible]	[illegible]	[illegible]	[illegible]	…9048
15	8.224188	-0.03438	0.568393	0.507649	0.269077	0.044201	0.582297	0.430838	0.		[illegible]	[illegible]	[illegible]	[illegible]	…3427
16	8.849125	0.552552	-0.07112	0.118488	-0.54963	0.549477	-0.15486	0.255883	-0		[illegible]	[illegible]	[illegible]	[illegible]	…5658
17	9.474063	-0.16921	-0.51845	-0.54874	0.034664	-0.25482	-0.49777	-0.54055	-0		[illegible]	[illegible]	[illegible]	[illegible]	…4547
18	10.099	-0.46792	0.257443	0.177541	0.508548	-0.42902	0.339458	0.02331	0		[illegible]	[illegible]	[illegible]	[illegible]	…2945
19	10.72394	0.33411	0.405309	0.434212	-0.30303	0.409068	0.348251	0.509125	-0		[illegible]	[illegible]	[illegible]	[illegible]	…7095
20	11.34888	0.329067	-0.39543	-0.40103	-0.32956	0.25661	-0.46045	-0.27454	-0		[illegible]	[illegible]	[illegible]	[illegible]	…5037
21	11.97381	-0.44179	-0.24736	-0.2075	0.467175	-0.4927	-0.15999	-0.35576	0.		[illegible]	[illegible]	[illegible]	[illegible]	…3475
22	12.59875	-0.1593	0.472914	0.49782	0.071966	-0.05964	0.506695	0.441648	0.		[illegible]	[illegible]	[illegible]	[illegible]	…2228
23	13.22369	0.485925	0.069281	-0.06239	-0.49104	0.499356	-0.03818	0.126592	-0		[illegible]	[illegible]	[illegible]	[illegible]	…5001
24	13.84863	-0.02108	-0.48369	-0.45077	0.189694	-0.13282	-0.47635	-0.49166	-0		[illegible]	[illegible]	[illegible]	[illegible]	…5668
25	14.47356	-0.46412	0.108059	0.299084	0.377338	-0.43492	0.219365	0.1206	0.468955		14.47356	-6.4380528	-6.34821	-6.24748	-6.29926
26	15.0985	0.187699	0.431223	0.279429	-0.38354	0.294142	0.377997	0.418479	-0.23107		15.0985	-6.5524631	-6.47463	-6.39404	-6.41083
27	15.72344	0.384162	-0.25689	-0.43557	-0.16654	0.311403	-0.3538	-0.32068	-0.34321		15.72344	-6.704496	-6.62624	-6.5336	-6.56338
28	16.34838	-0.31179	-0.32677	-0.04852	0.453374	-0.395	-0.23623	-0.25122	0.384802		16.34838	-6.9038367	-6.82141	-6.74021	-6.75337
29	16.97331	-0.26093	0.360844	0.442756	-0.07399	-0.15371	0.426633	0.429082	0.144442		16.97331	-7.0269589	-6.95708	-6.86887	-6.883
30	17.59825	0.395481	0.187561	-0.18573	-0.4006	0.440422	0.067756	0.033217	-0.44378		17.59825	-7.1763898	-7.10013	-7.02103	-7.0324
31	18.22319	0.112546	-0.41656	-0.3328	0.280904	-0.01642	-0.43901	-0.4325	0.077077		18.22319	-7.3003896	-7.22016	-7.14443	-7.14442
32	18.84813	-0.42377	-0.03406	0.353548	0.241934	-0.42058	0.099168	0.178949	0.39348		18.84813	-7.4293571	-7.36297	-7.28814	-7.28509
33	19.47306	0.041619	0.416134	0.138461	-0.39912	0.173408	0.38815	0.332216	-0.26653		19.47306	-7.5721078	-7.48447	-7.42968	-7.41346

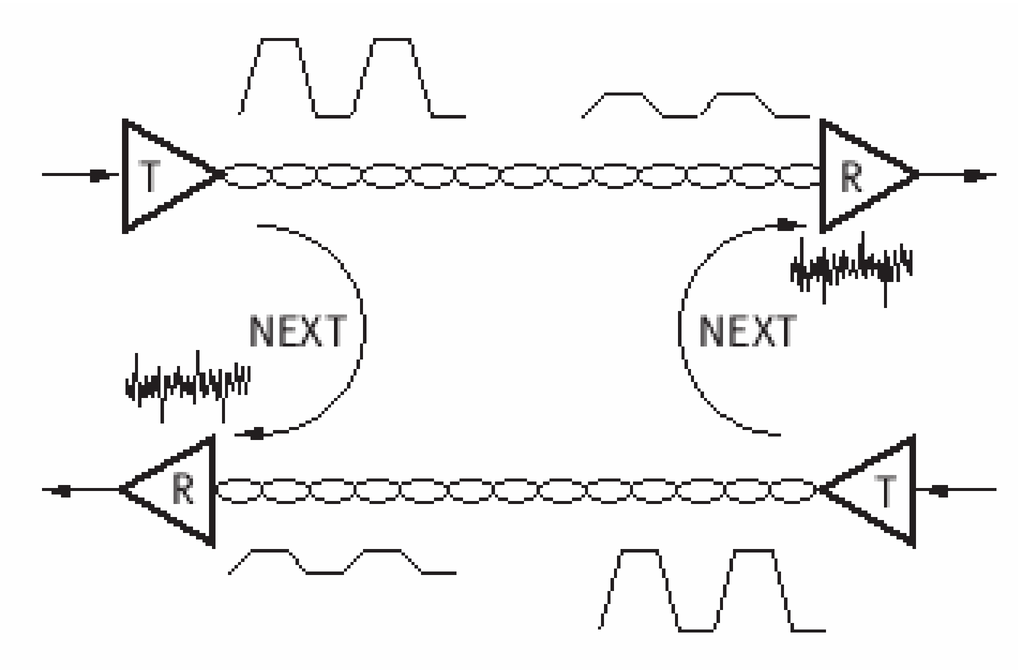
IL Cat 6 (55m) / IL Cat 6 (100m) / IL Cat 7 (100m) / NEXT / ELFEXT / Return Loss / ANEXT 47 / ANEXT 60 / ANEXT 62



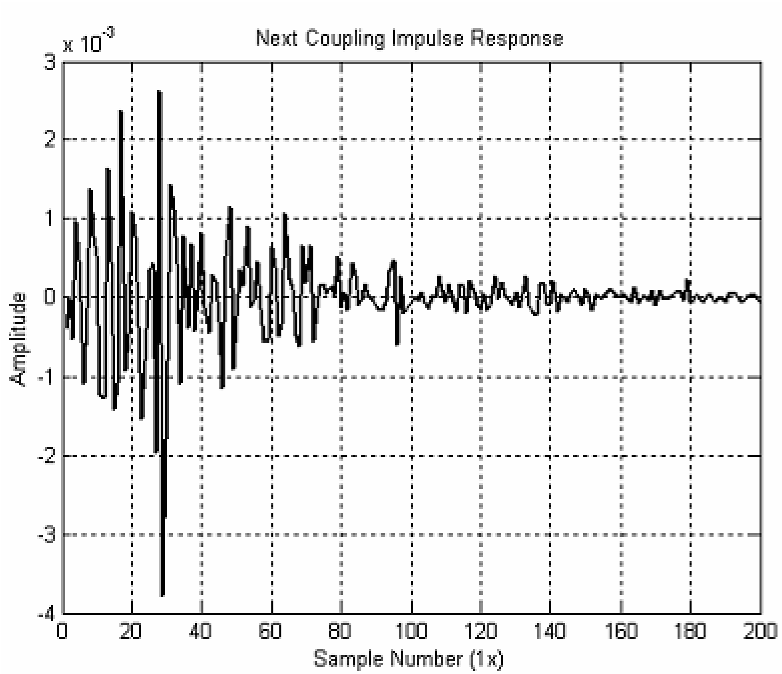
Insertion Loss



NEXT

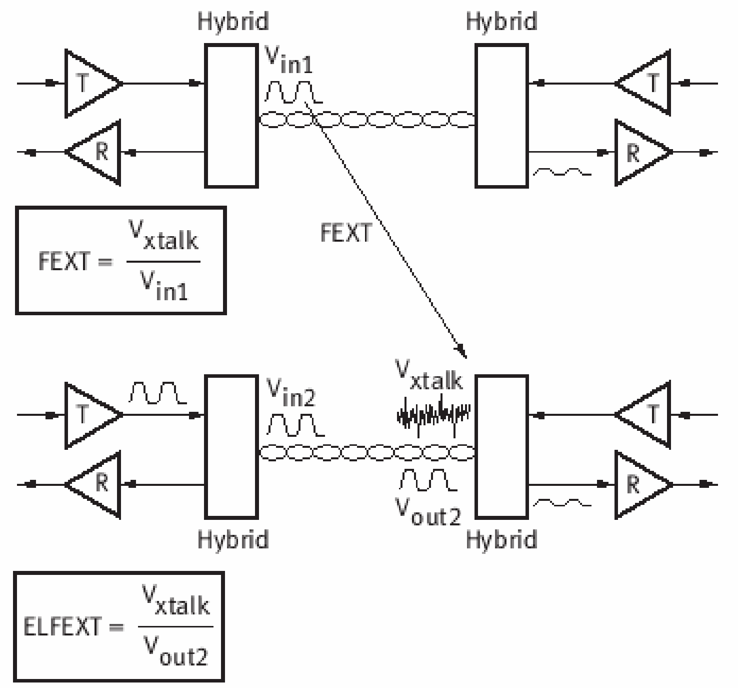


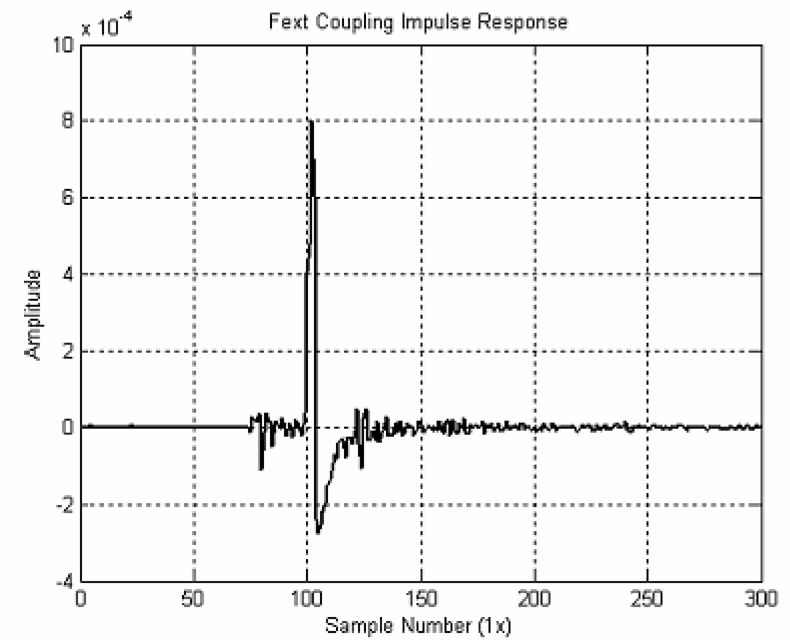
T
R
NEXT
NEXT
R
T



Next Coupling Impulse Response
x 10^-3
Amplitude
Sample Number (1x)
3
2
1
0
-1
-2
-3
-4
0
20
40
60
80
100
120
140
160
180
200

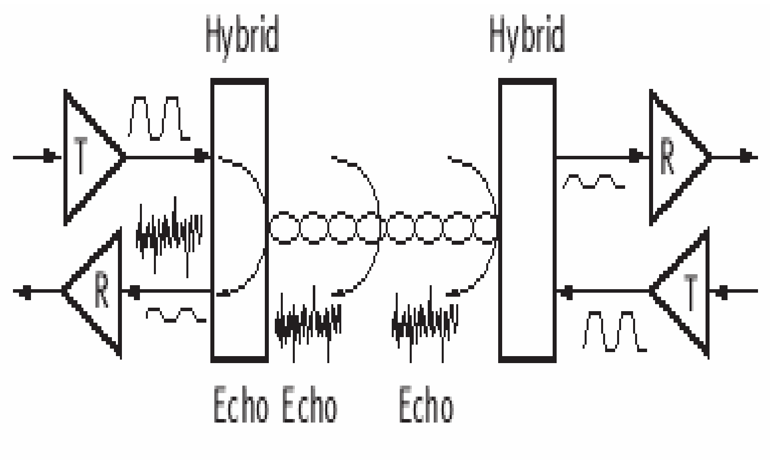
FEXT/ELFEXT

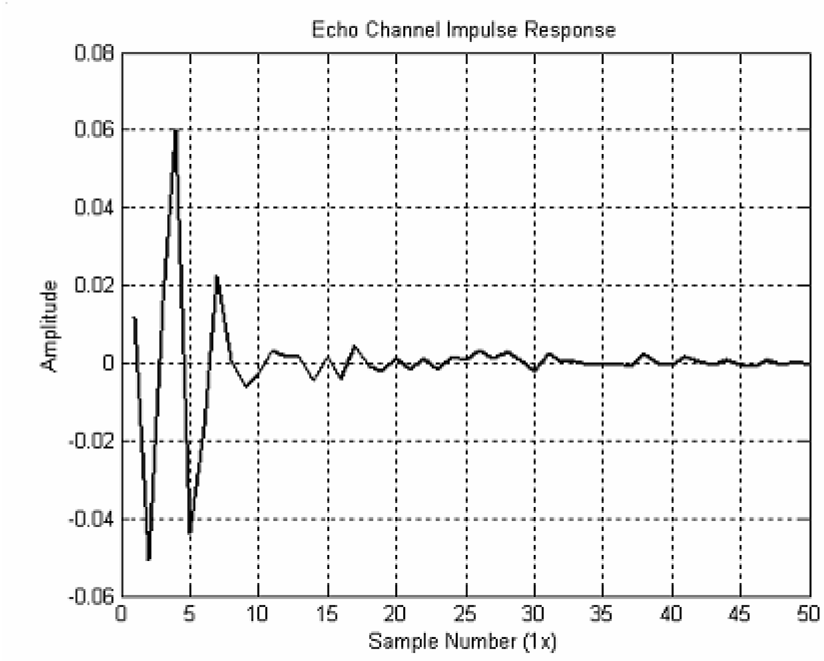

Hybrid
Hybrid
V_{in1}
T
R
T
R
FEXT = $\frac{V_{xtalk}}{V_{in1}}$
FEXT
V_{xtalk}
T
V_{in2}
T
R
R
V_{out2}
Hybrid
Hybrid
ELFEXT = $\frac{V_{xtalk}}{V_{out2}}$


Fext Coupling Impulse Response
x 10^{-4}
Amplitude
Sample Number (1x)
10
8
6
4
2
0
-2
-4
0
50
100
150
200
250
300

Echo

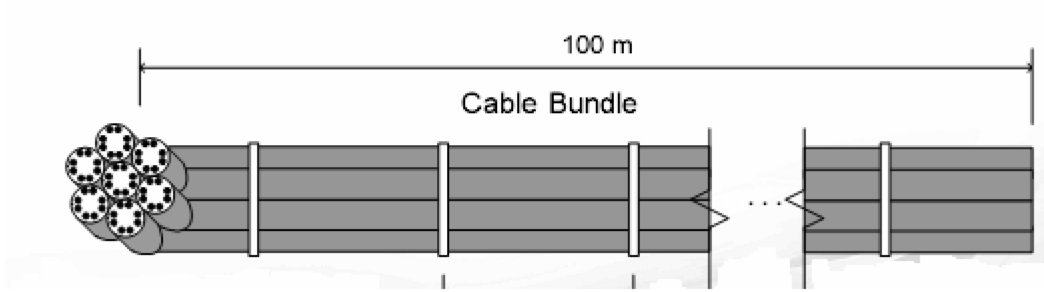
- Near-end Echo / Far-end Echo

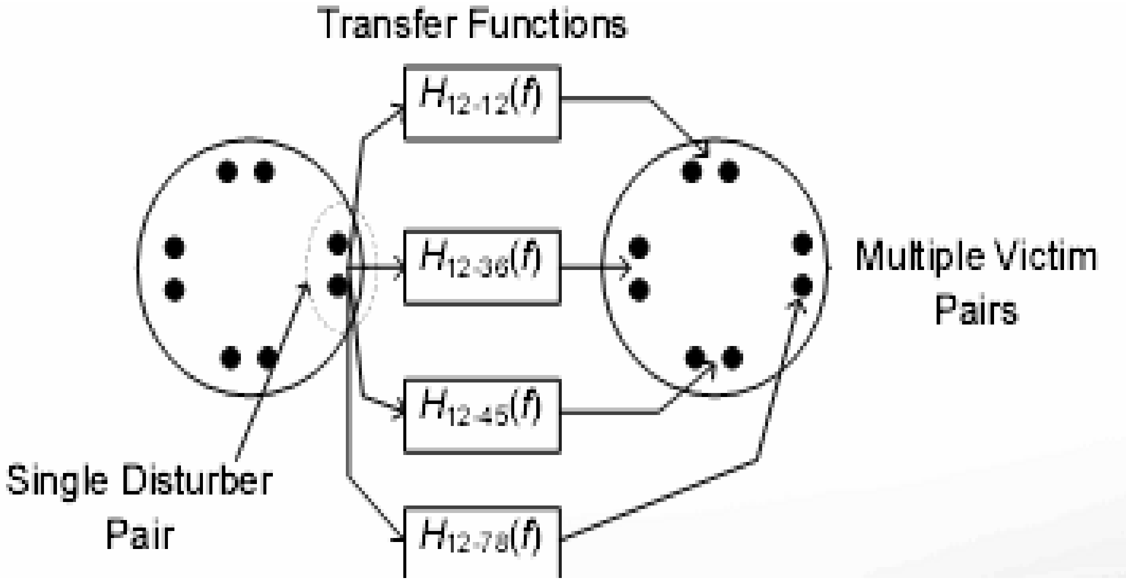




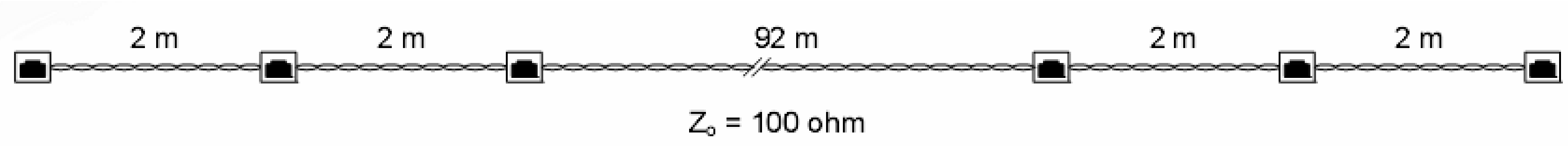
Alien Crosstalk

- Characterize as "power sum"

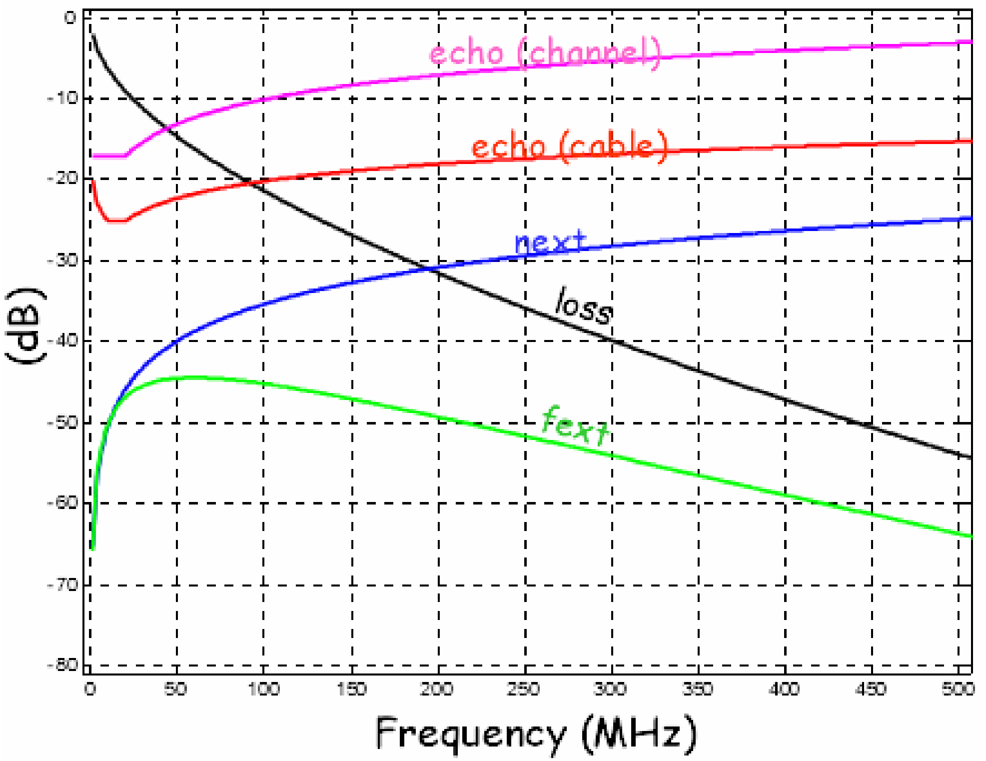




Impairment Frequency Response



- Cable manufacturers guarantee cable performance using frequency domain “limit lines”
- No phase information
- Measurements needed to model in simulations

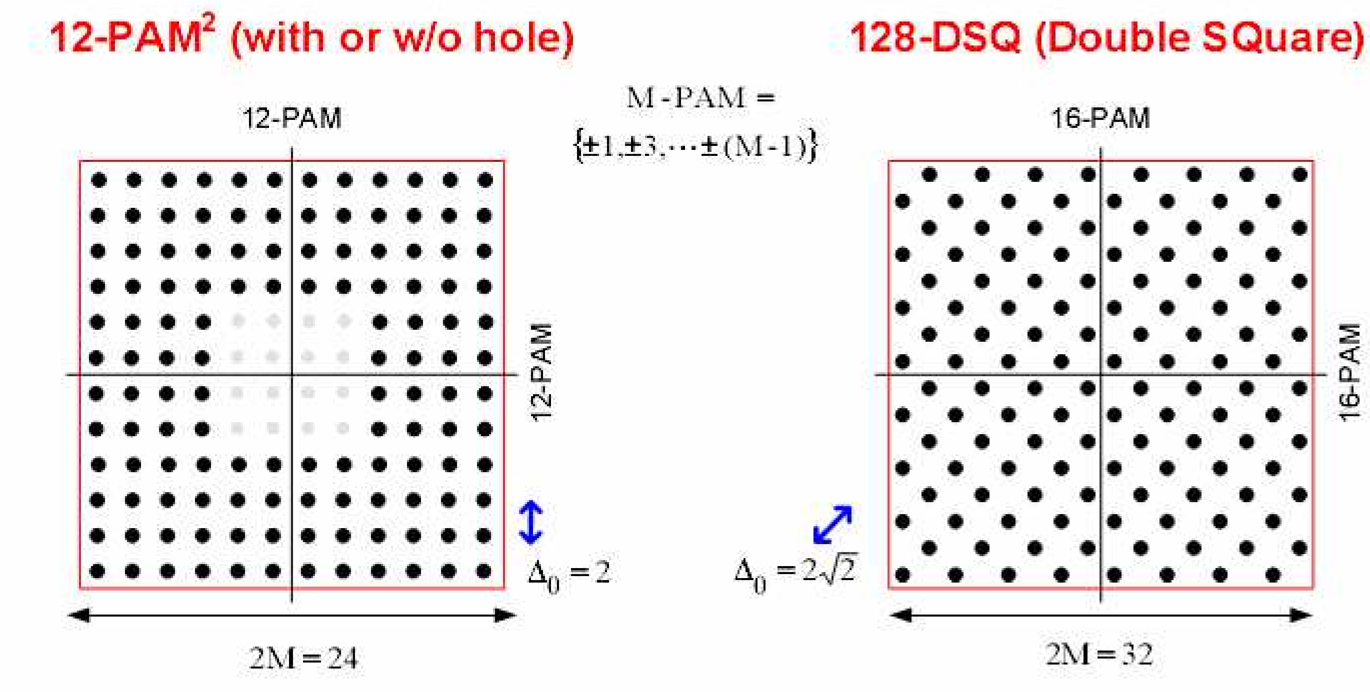


Coding & Modulation

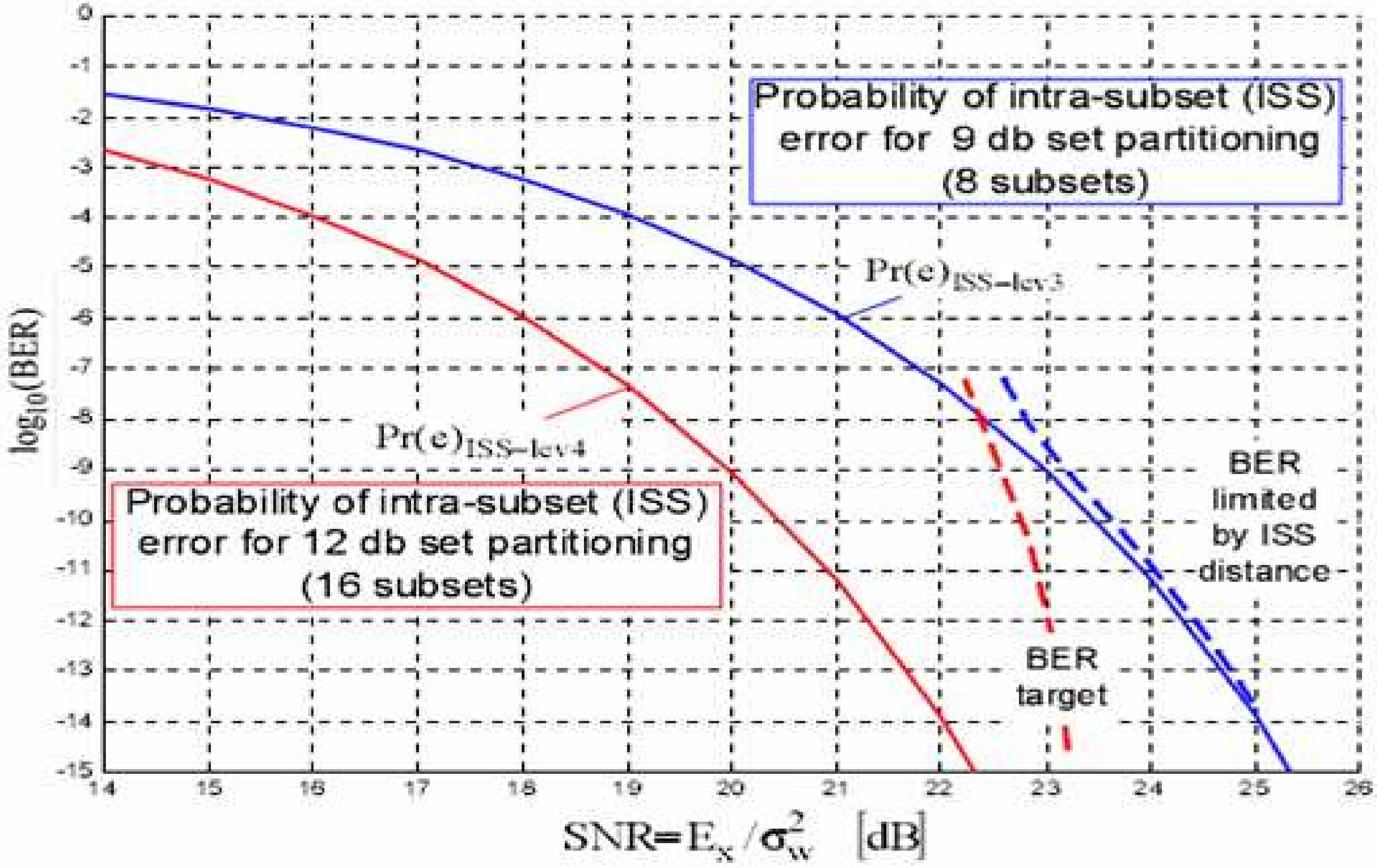
- DSQ vs PAM-12 modulation
- Coded modulation with LDPC
- 128-DSQ bit-mapping
- 128-DSQ soft De-mapping
- Coding and framing for 128-DSQ
- Performance of 128DSQ with LDPC(2048,1723)

DSQ vs 12-PAM Modulatoin

- Using coded modulation
- 2D-constellations (DSQ-128 vs 12-PAM^2)



BER for intra-subset (Uncoded bits)=> To choose minimum distance in a subset

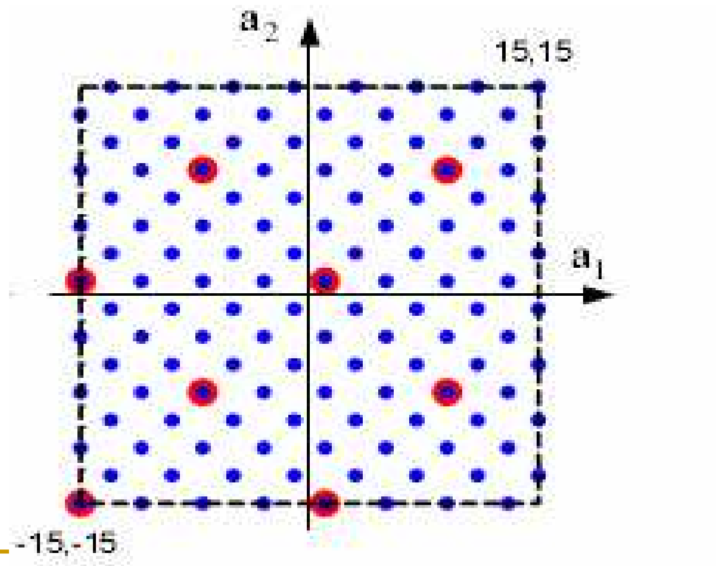


$$\mathbf{128-DSQ}: M=16;\ E_x=(2M)^2/12;\ \Delta_0^2=8$$

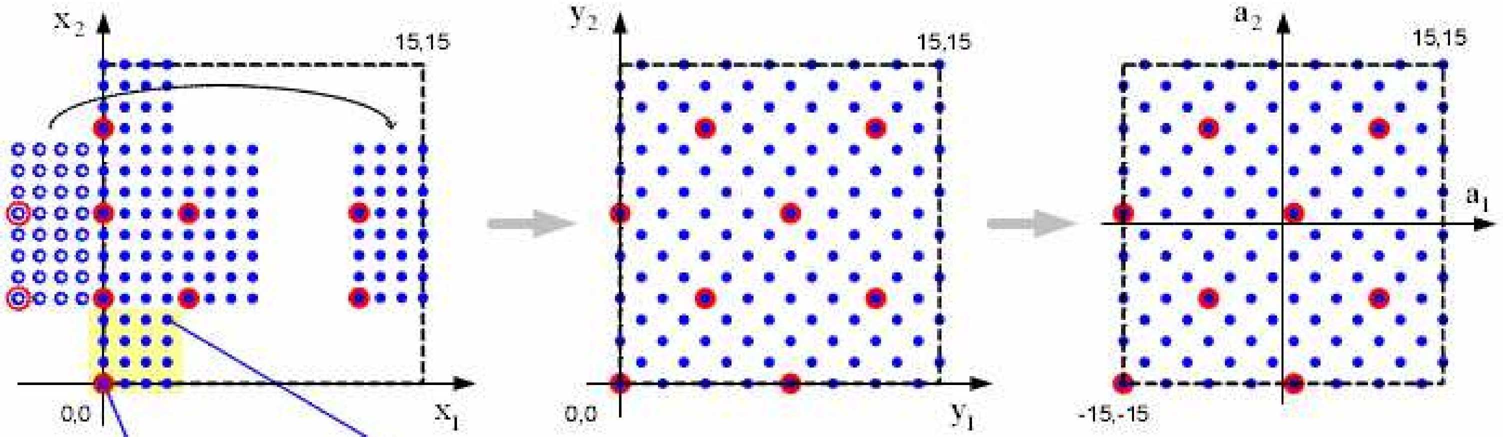
$$\Delta_3^2=8\Delta_0^2:\ \Pr(e)_{ISS-lev3}=\frac{1}{2}\times 4\times Q\left(\frac{\Delta_3}{2\sigma_w}\right);\ \Delta_4^2=16\Delta_0^2:\ \Pr(e)_{ISS-lev4}=\frac{1}{2}\times 4\times Q\left(\frac{\Delta_4}{2\sigma_w}\right)$$

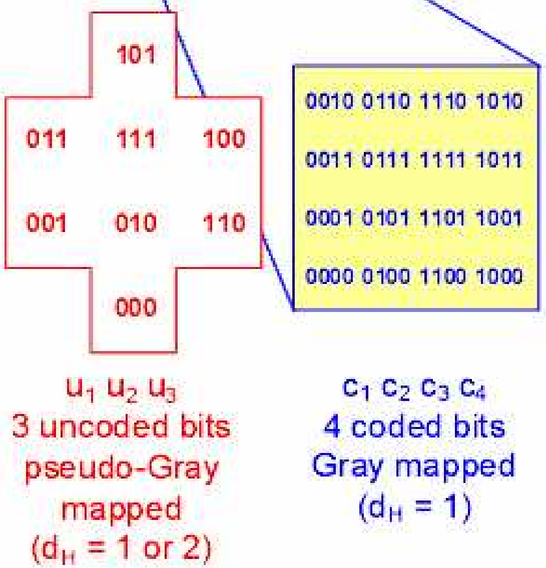
Coded-modulation with LDPC

- 12db set partition (Distance is $4\Delta_0$ in a subset)
- 16 subset (Using 4 LDPC encoded bits to choose which subset)
- Every subset has 8 symbols (3 uncoded bits)



128-DSQ bit-mapping(1/2)





Step 1: $0 \le (x_i = 8x_i^3 + 4x_i^2 + 2x_i^1 + x_i^0) \le 15, \quad i = 1,2$

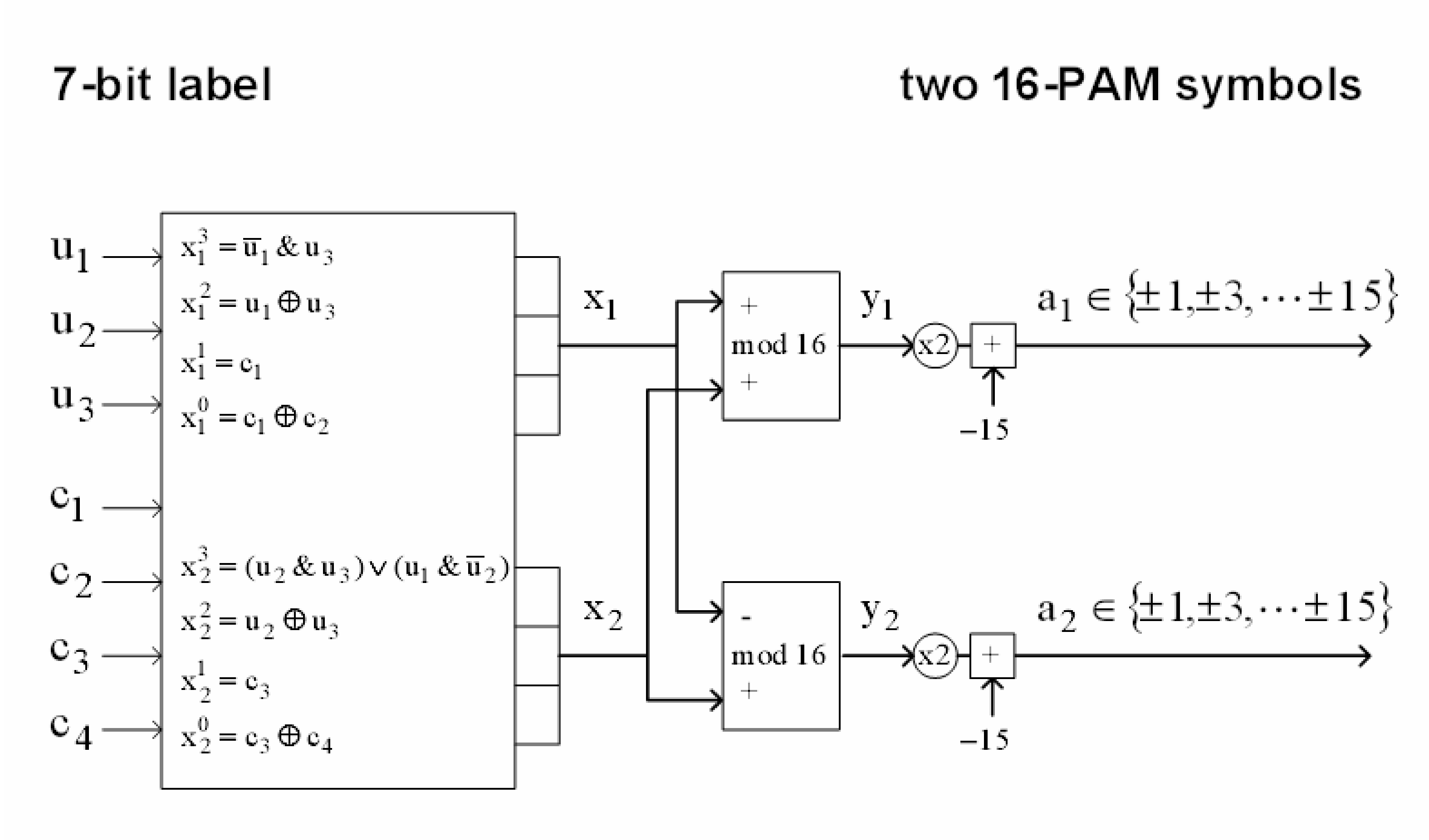
$$x_1^3 = \bar{u}_1 \,\&\, u_3 \qquad x_2^3 = (u_2 \,\&\, u_3) \vee (u_1 \,\&\, \bar{u}_2)$$
$$x_1^2 = u_1 \oplus u_3 \qquad x_2^2 = u_2 \oplus u_3$$

$$x_1^1 = c_1 \qquad x_2^1 = c_3$$
$$x_1^0 = c_1 \oplus c_2 \qquad x_2^0 = c_3 \oplus c_4$$

Step 2: $\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \overbrace{\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix}}^{\mathbf{R}} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \bmod 16$

Step 3: $\begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = 2\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} - \begin{bmatrix} 15 \\ 15 \end{bmatrix}$

128-DSQ bit-mapping(2/2)



128-DSQ Soft De-mapping for 4-coded bits

- Using two received 16-PAM symbol (One DSQ symbol) to generate **four initial values** for 4-coded bits used in LDPC decoding

$$\mathrm{llrb}(x) = \ln \frac{\sum_k \exp\left(-[x-(4k+0)]^2/2\sigma^2\right) + \exp\left(-[x-(4k+1)]^2/2\sigma^2\right)}{\sum_k \exp\left(-[x-(4k+2)]^2/2\sigma^2\right) + \exp\left(-[x-(4k+3)]^2/2\sigma^2\right)} \cong \frac{1}{\sigma^2}\begin{cases} x+0.5 & : \; 0 \le x \le 0.5 \\ 1.5-x & : \; 0.5 \le x \le 2.5 \\ x-3.5 & : \; 2.5 \le x \le 4 \end{cases}$$

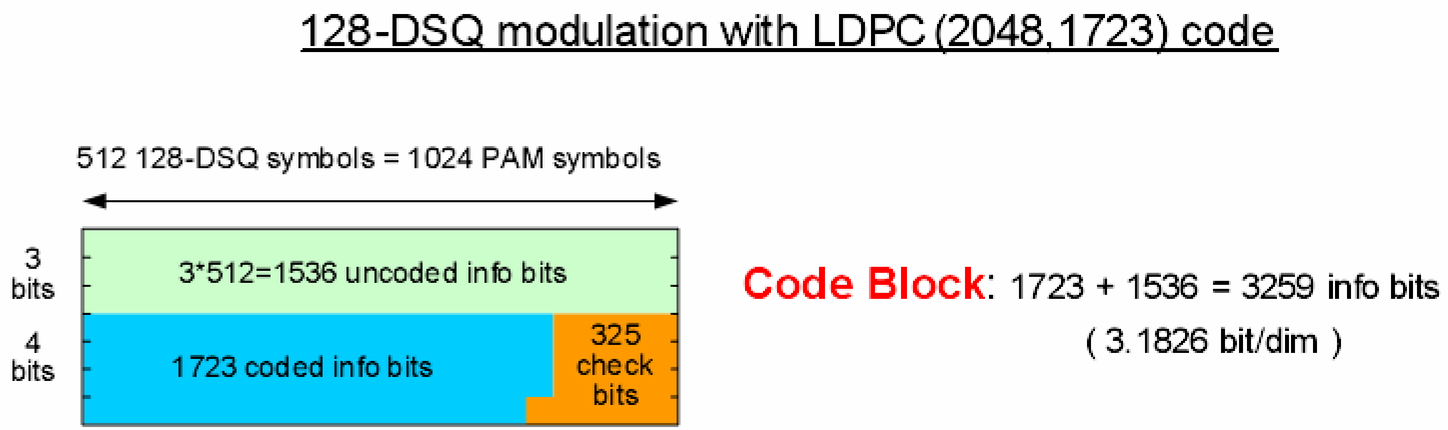
$$\overbrace{\begin{bmatrix} 0.5 & -0.5 \\ 0.5 & 0.5 \end{bmatrix}}^{\mathbf{R}^{-1}} \begin{bmatrix} (s_1+15)/2 \\ (s_2+15)/2 \end{bmatrix} = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

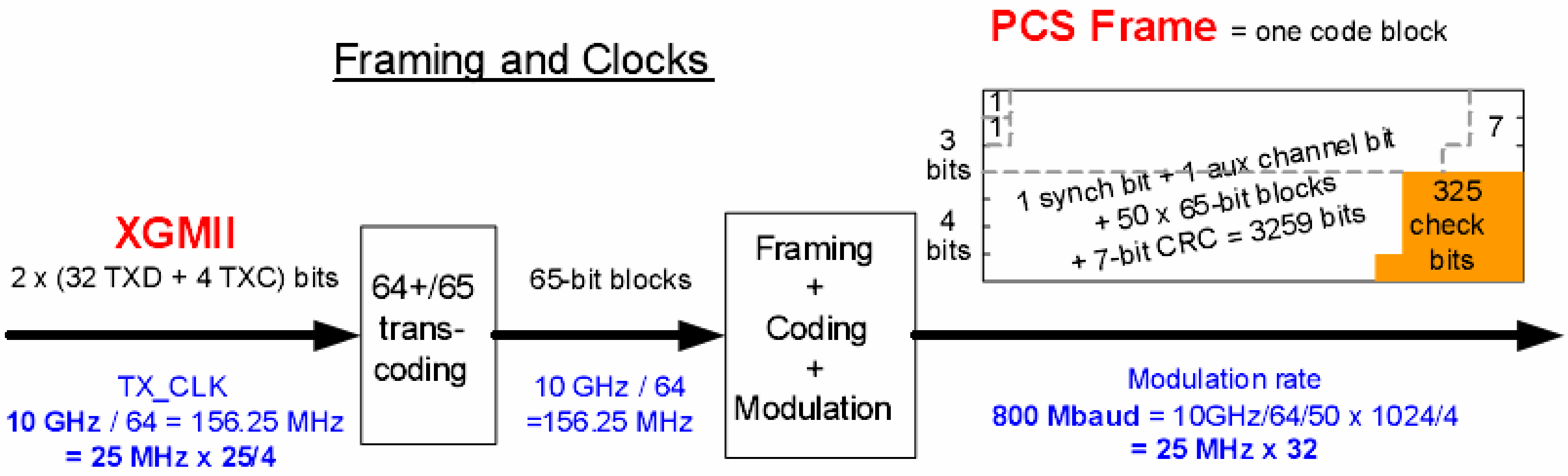
=>

$$\log\frac{\Pr(c_1=0/x_1)}{\Pr(c_1=1/x_1)} = \mathrm{llrb}(x_1 \bmod 4) \qquad \log\frac{\Pr(c_2=0/x_1)}{\Pr(c_2=1/x_1)} = \mathrm{llrb}(x_1+1 \bmod 4)$$

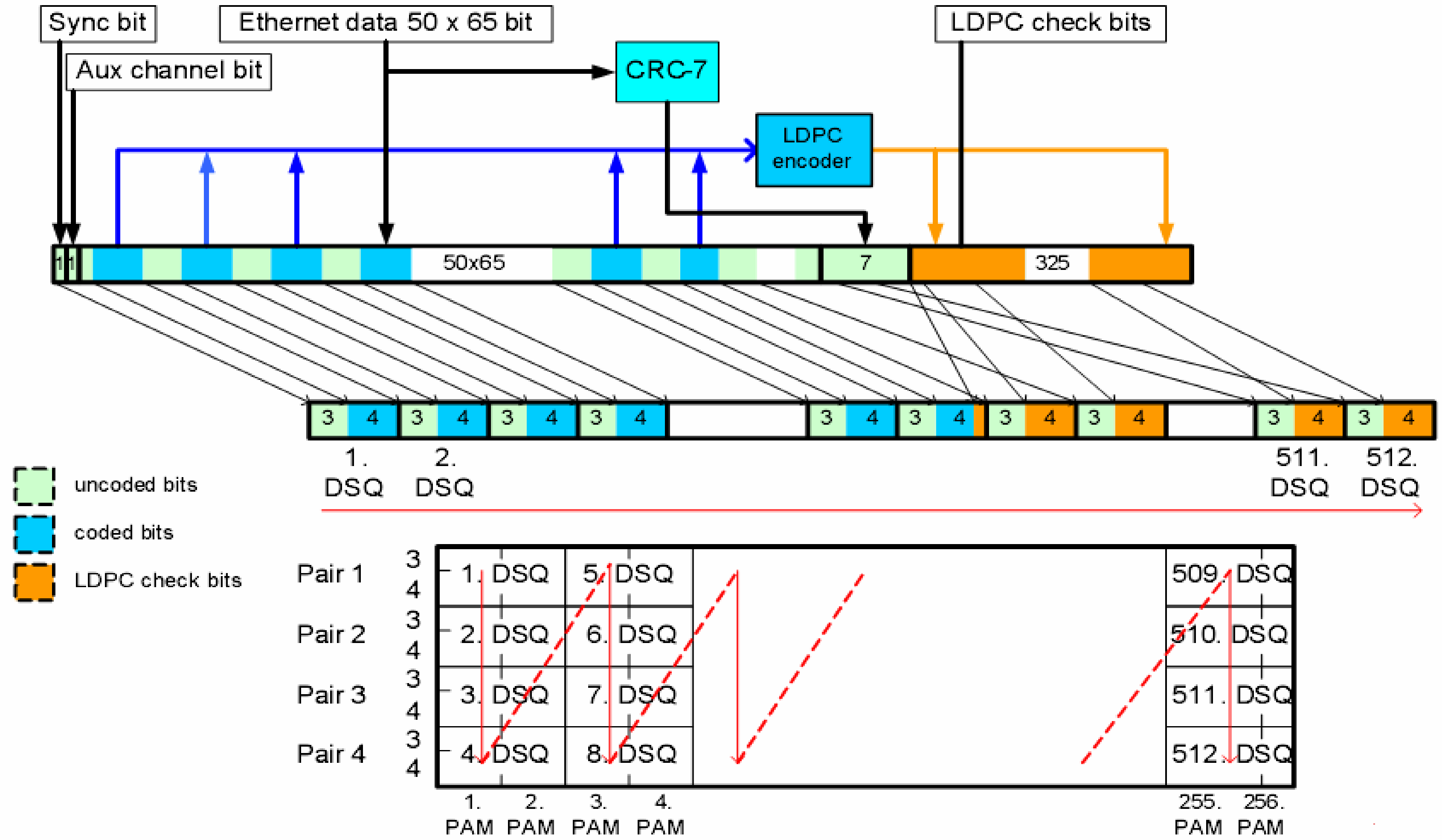
$$\log\frac{\Pr(c_3=0/x_2)}{\Pr(c_3=1/x_2)} = \mathrm{llrb}(x_2 \bmod 4) \qquad \log\frac{\Pr(c_4=0/x_2)}{\Pr(c_4=1/x_2)} = \mathrm{llrb}(x_2+1 \bmod 4)$$

Coding and framing for 128-DSQ





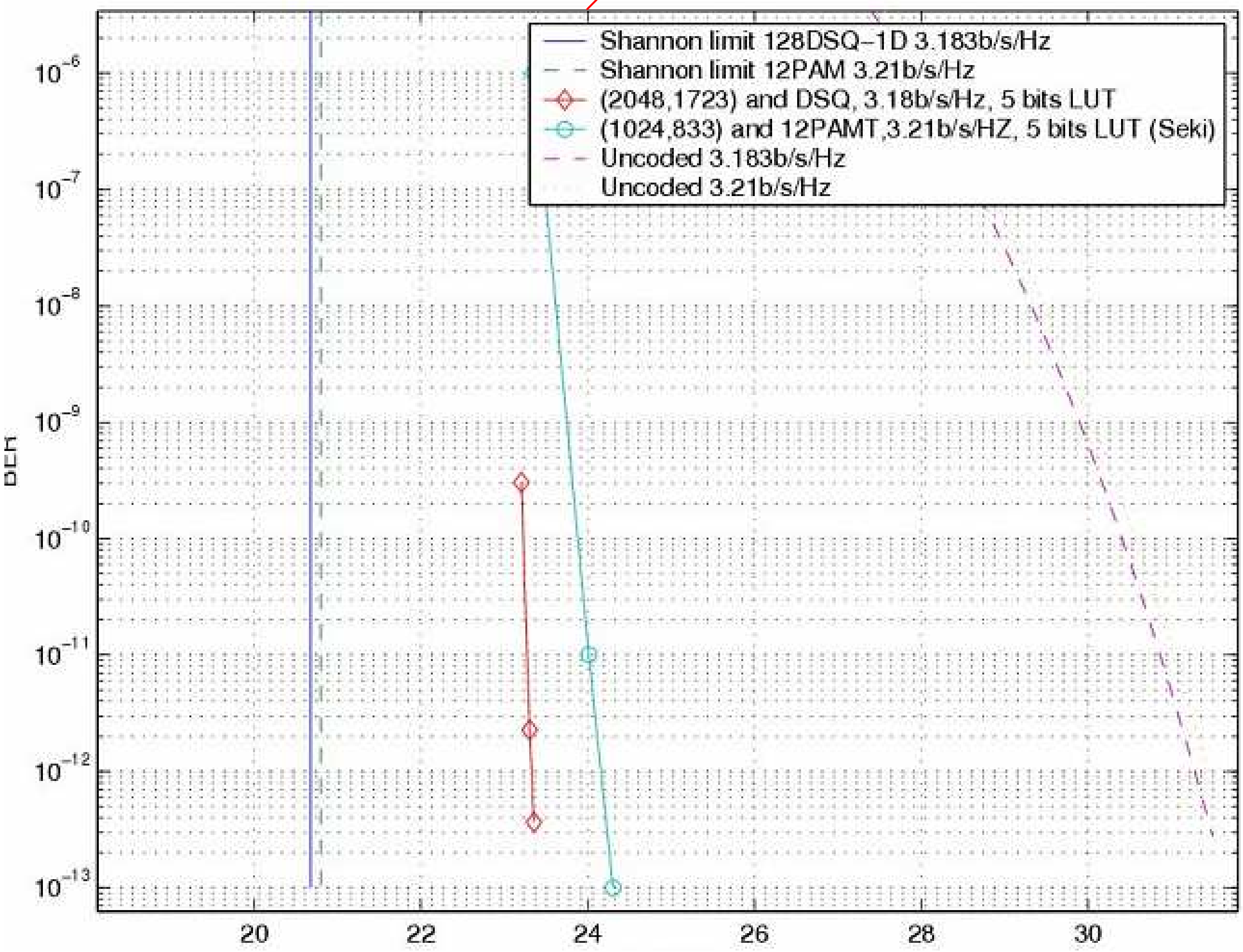
Framing details : 128DSQ + LDPC(2048,1723)



(Alternatively, use symbol interleavings of various kinds)

128DSQ + LDPC(2048,1723) performance

System require SNR 23.4 dB



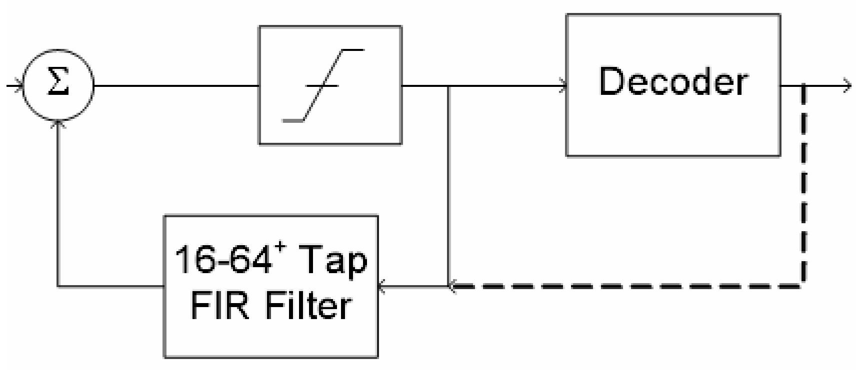
- BER = 10^{-12} at SNR = 23.32dB
- 5-bit look up table
- Final point at SNR = 23.35dB: 2.184e13 bits simulated with 1 block error
- 128DSQ mapping as described in ungerboeck_1_1104.pdf and ungerboeck_2_0904.pdf
- G and H matrices as defined in 802.3an public area

Equalization

- Channel equalization via DFE ?
- Decoupling FEC from equalization (THP)
- Tx-based equalization
- Fundamental benefits of precoding
- Precoder adaptation ?
- Precoder architecture (IIR or FIR) ?

Channel equalization via DFE ?

- **DFE cannot separate from channel coding**
  - Error propagation substantially reduces coding gain
  - Zero delay decisions irreconcilable with basic idea of channel coding

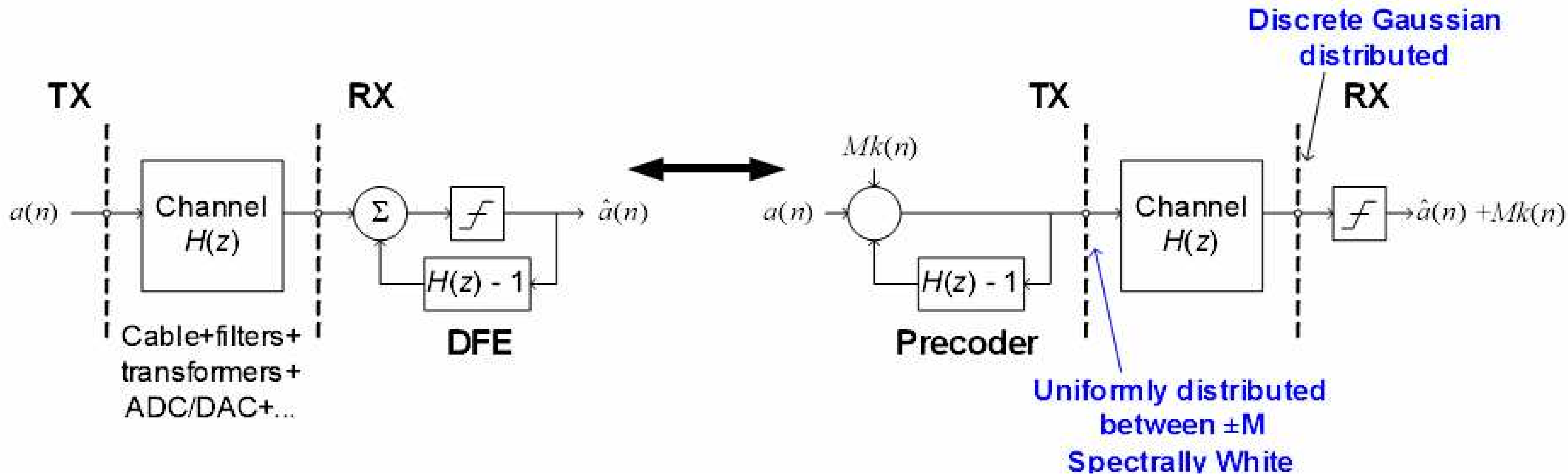


- **Usually require placing some portion of decoder inside the feedback loop (DFSE)**
  - **DFSE ➔** combine Viterbi decoder with slicer to reduce decision error (Used in 1000Base-T)
  - Introduces a critical timing path

    ➔ limits max baud rate
  - Incompatible with high performance block or iterative codes

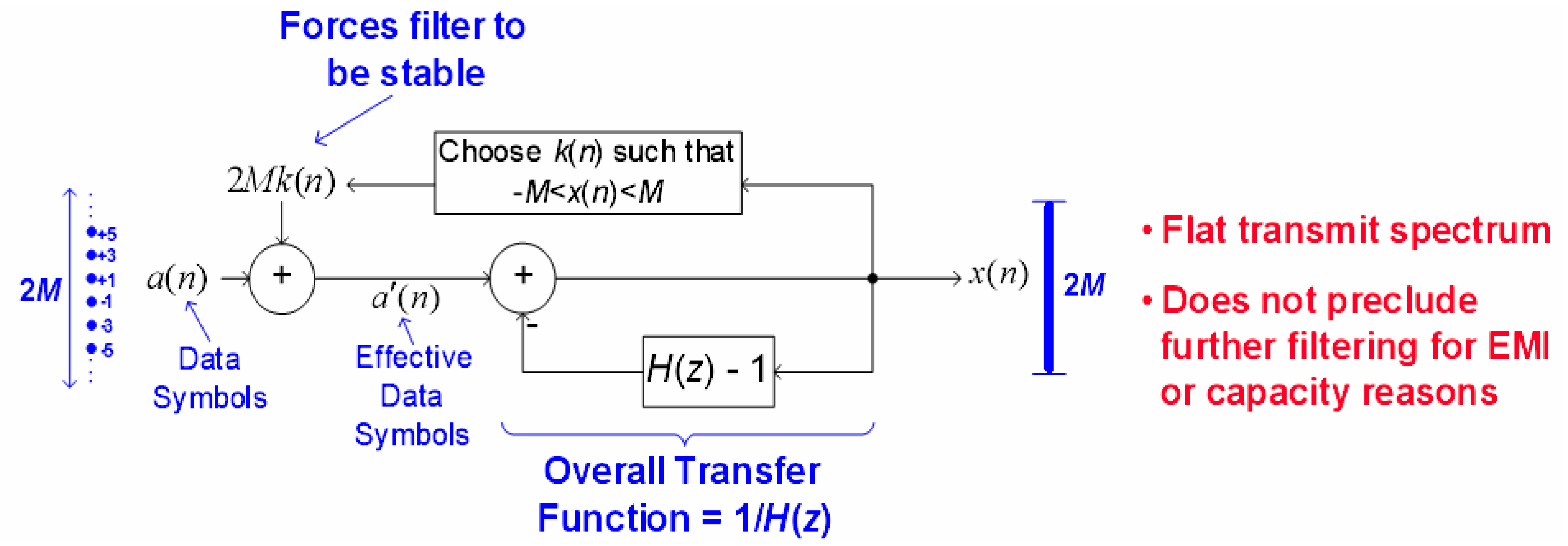
Decoupling FEC from equalization

- **Precoding is a well-known technique for decoupling channel equalization from channel coding**
  - Move DFE from RX to TX
  - Necessary for LDPC or concatenated coding schemes



Tx-Based Equalization

- Moveing postcusor equalization from receiver to the transmitter
- Achieveing similar performance as DFE with correct decision
  - Precoding feedback symbols are known , not estimated
  - Equalization is independent of channel coding performance

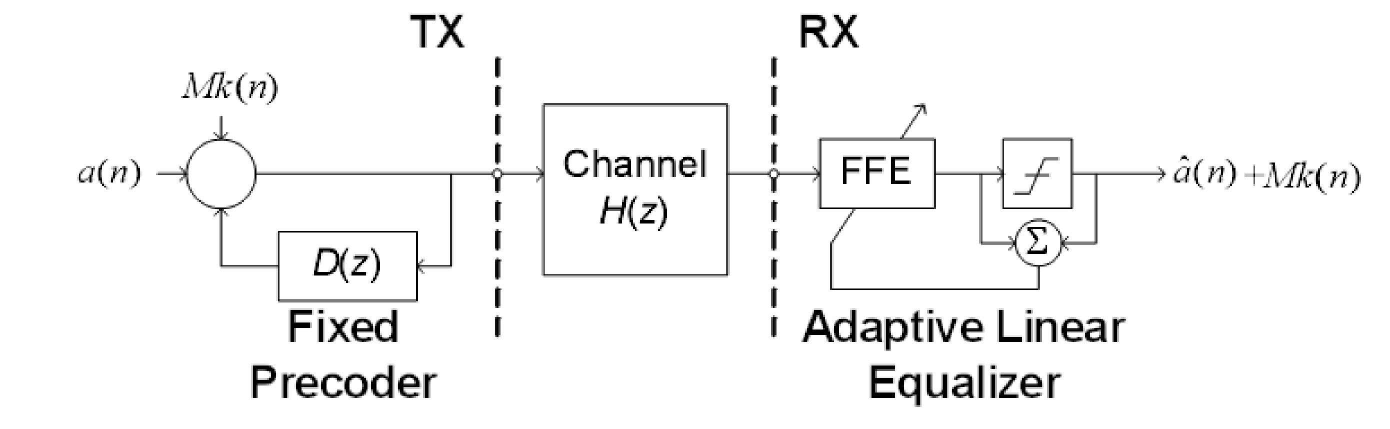


Fundamental benefits of Precoding

- Permits more powerful channel codes required to meet 10Gbps
  - Decouples equalization from channel coding
- Retains asymptotic optimality of decision feedback equalization without error propagation
- Does not affect transmitted spectrum (EMI)
  - Does not preclude any form of transmit filtering
- Removes DFSE timing loop – simplifies timing closure

Precoder adaptation not necessary ?

- **Programmable precoding**
  - Precoder coefficients chosen at start-up to approximately match channel response
  - Adaptive linear RX removes residual ISI



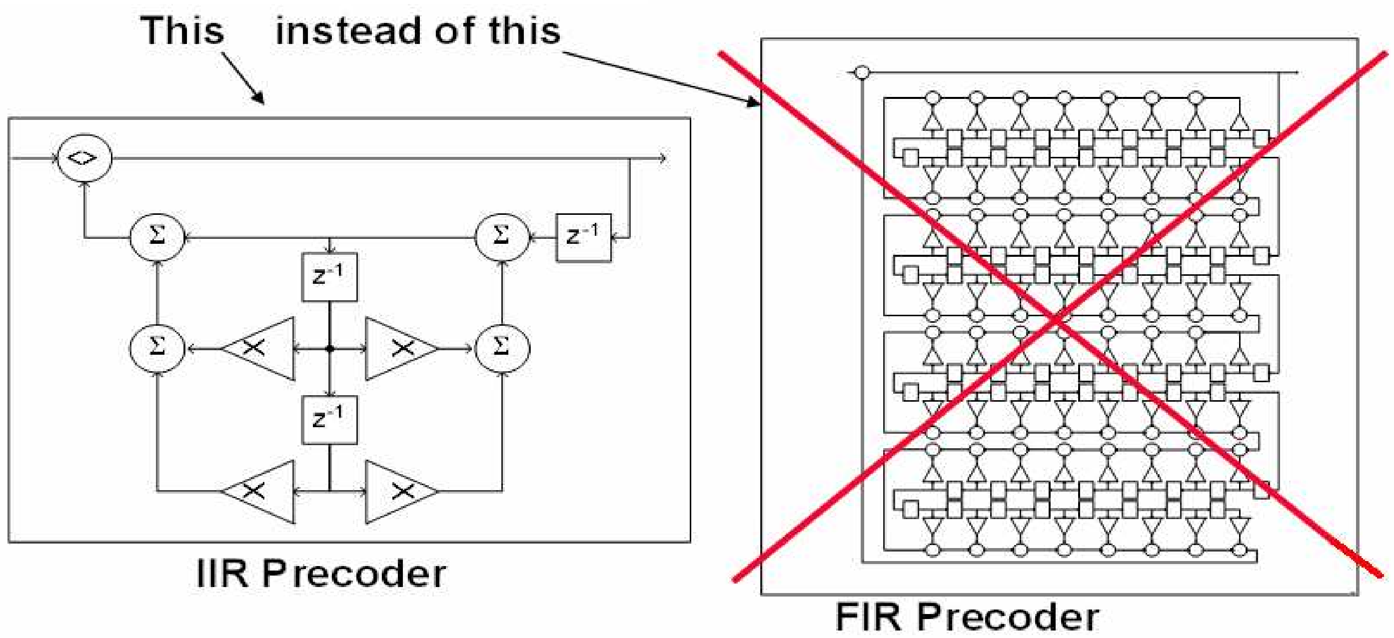
- **Coefficients are a function of cable length**
  - Pre-store in a small cable-length

Number of Precoder coefficients reduced over 10x with IIR model

- Over all channel is accurately modeled by 2nd order IIR

$$H(z) = \frac{(1 - z^{-1})(1 + \delta z^{-1})}{1 - \alpha z^{-1} + \beta z^{-2}}$$

Only 3 coefficients

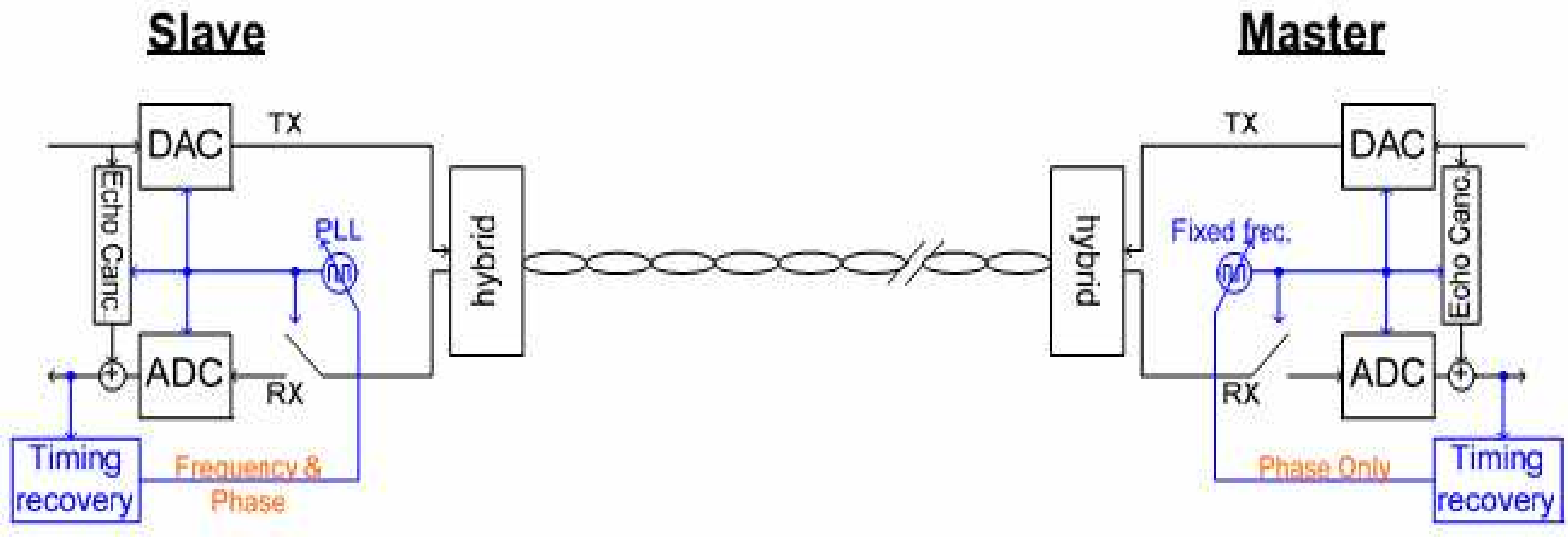


Timing recovery

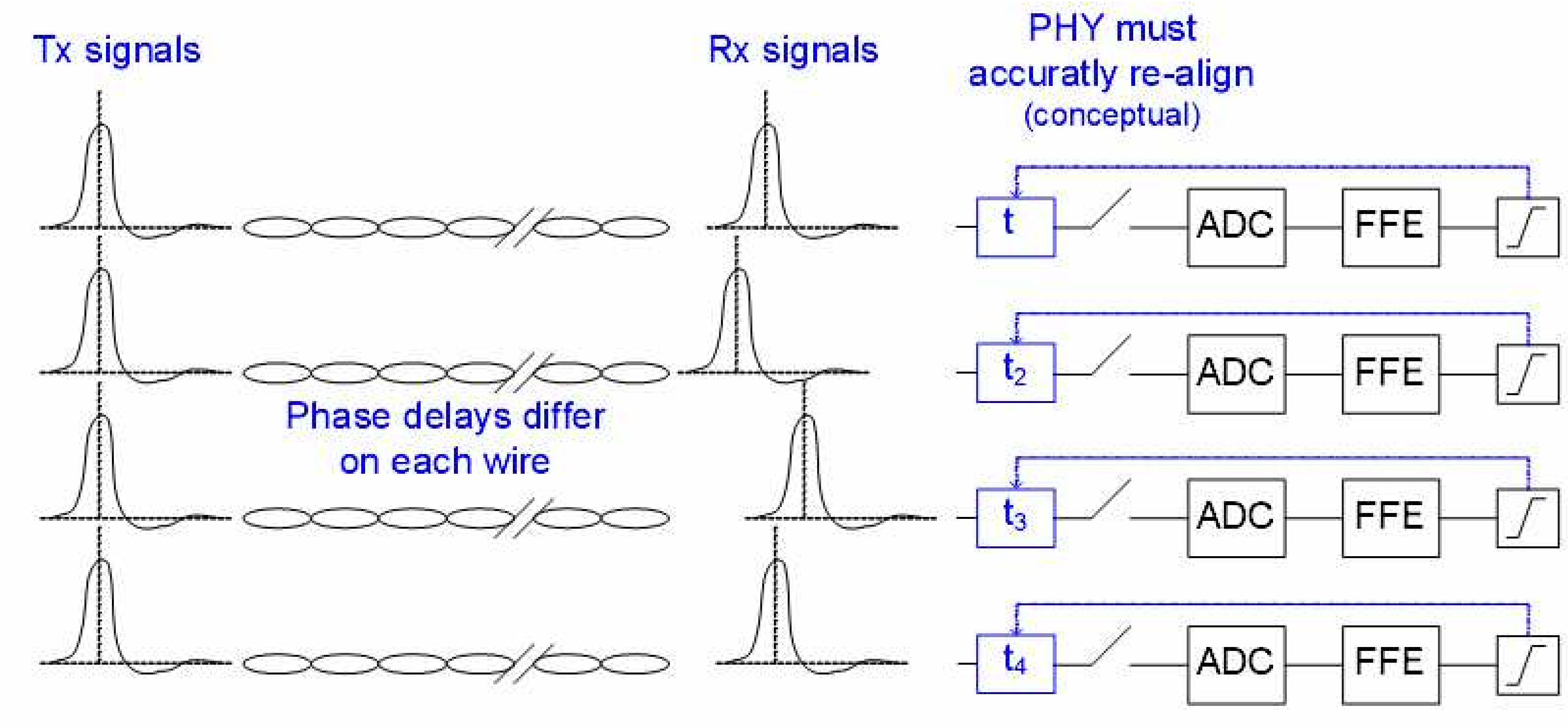
- Loop Timing
- Multiphase VCO approach
- Digital interpolation approach

Loop Timing

- Echo & NEXT cancellation generally require the transmitter and receiver to be clocked from the same source



Traditional Analog/Digital Phase Compensation Concept

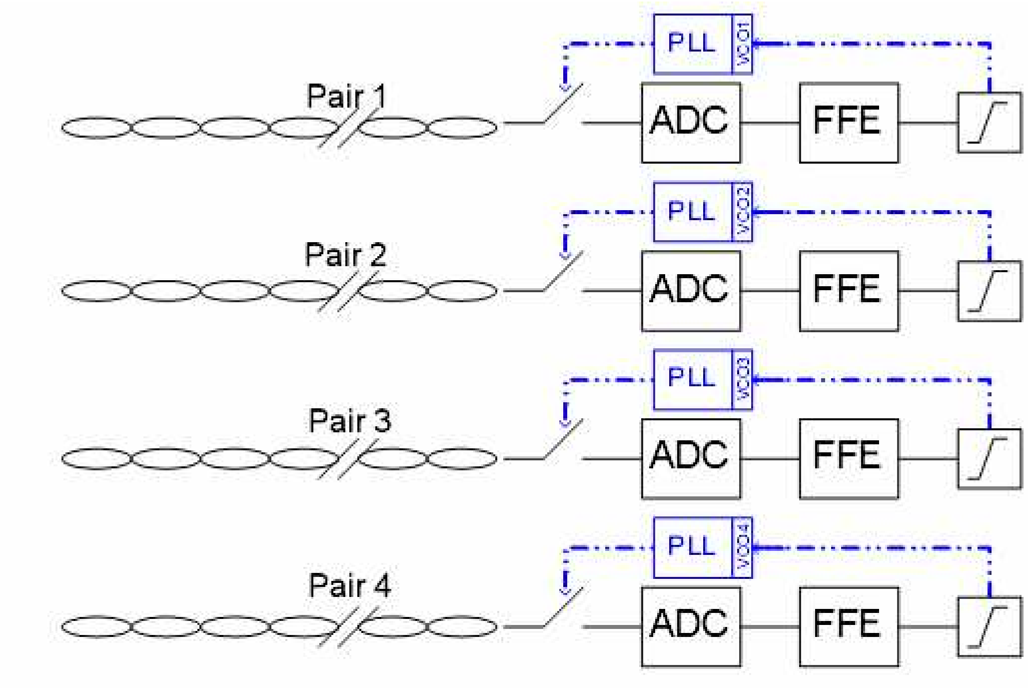


- optimal baud spaced samples are at pulse peak
- independently adjust phase for each channel

4-channel sampling approaches

- Appro. 1：independent PLL per channel
- Appro. 2：single VCO with phase selector
- Appro. 3 ：Digital interpolator instead of analog VCO or phase selector (Free running clock for ADC)

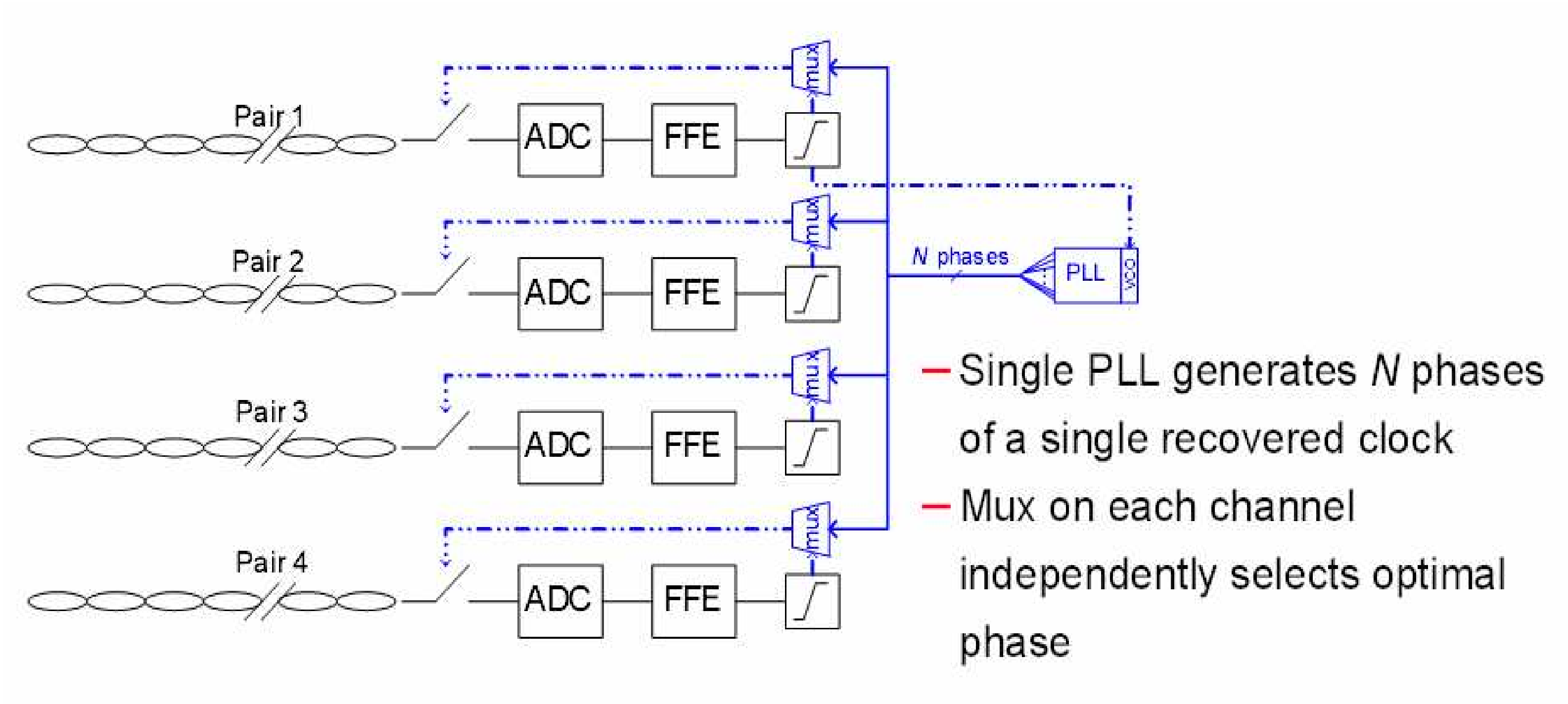
Independent PLL per channel



– Each PLL independently adapts to optimal frequency/phase

- **Theoretically possible but has implementation challenges**
  - Difficulties with multiple VCOs on the same die – interactions almost inevitable
  - Injection locking has been shown to be the root cause failure mechanism in previous product

Single VCO with phase selector (1/2)



- Phase-step cause echo cancellation errors
- 50-60 dB echo cancellation requires very large number of phases

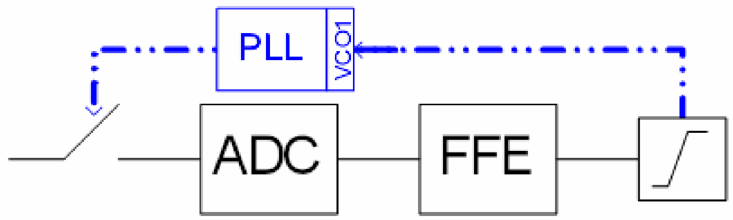
  ➔Number of 10G >> Number of 1G

Single VCO with phase selector (2/2)

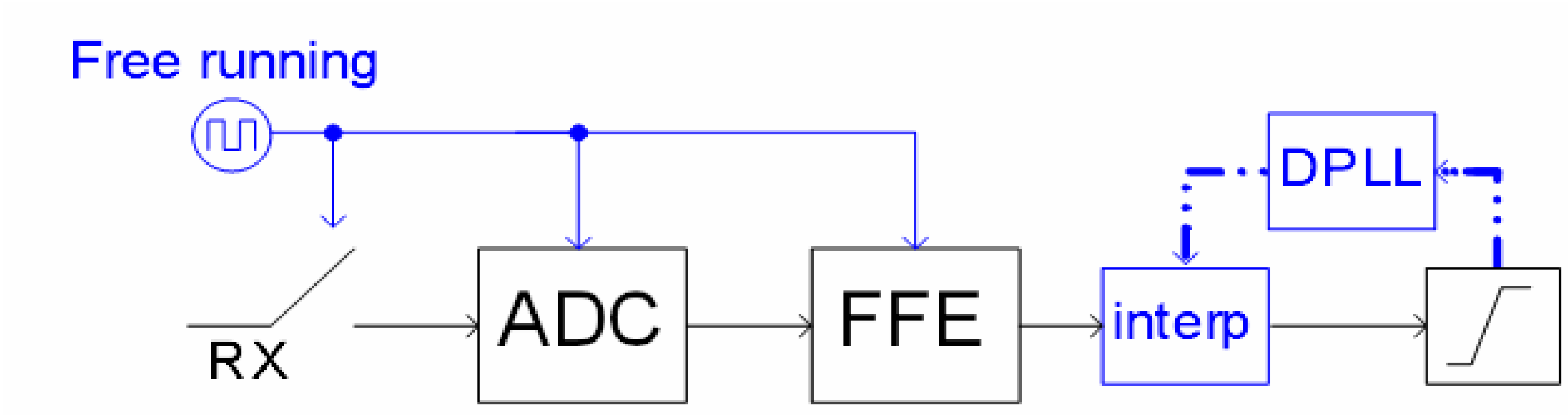
- **Implementation challenge**
  - High precision phase selector
  - Latency (ADC+FFE) in PLL loop
  - Low jitter requirement may constrain design options for ADC ,FFE , Slicer
  - Trade off between jitter tolerance and latency

    ➔Jitter tolerance requires PLL bandwidth to be increased

    ➔Latency requires PLL bandwidth to be reduced



Free running clock / Digital interpolation (1/3)



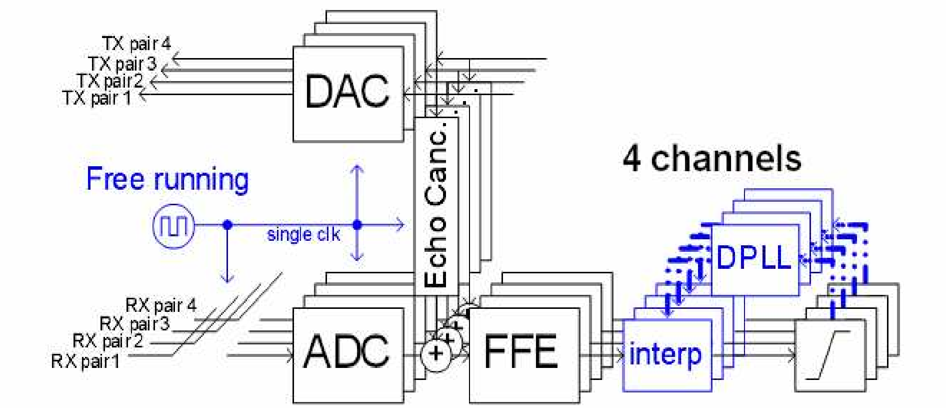
- ADC / FFE clock at the same free running clock
- Moving timing recovery after FFE

Free running clock / Digital interpolation (2/3) [Advantage of this way]

- Remove latency restriction on ADC and FFE
  -- open opportunity for design innovation

- Free running clock removes requirement for high precision phase selector

- ADC , DAC , FFE , Echo canceller all on the same clock
  -- remove need for FIFOs

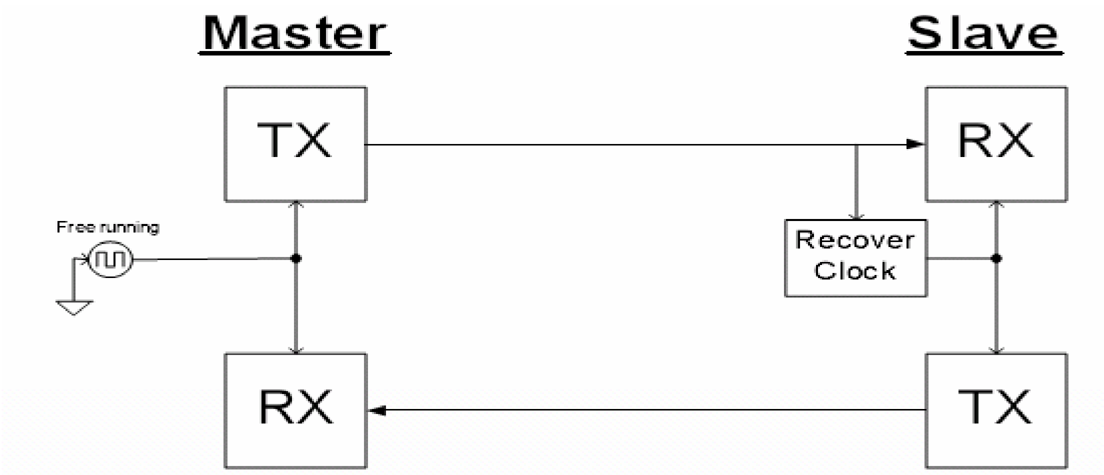


- Analog PLL per channel not required , single clock for 4 channel

Free running clock / Digital interpolation (3/3) [Implementation challenge]

- Baud rate sampling with zero excess bandwidth
  - When ADC samples with free running clock, we need Nyquist rate sampling or oversampling to recover the signal
    ➔ Limits transmitted BW <= (1/2T) when samples at baud rate .

- Slave optionally transmits with recovered clock
  - Permits single free running clock at both end .



Transmitter front-end solutions

- Linearity specification
- SNR margin vs TX voltage
- TX bandwidth -- Zero excess bandwidth is desired
- TX PSD proposal
- Transmitter front-end

  ➔Digital oversampling(2X) filter vs.

  Analog transmitting filter

Linearity specification

- Two measurement index
  - SFDR (dB) (Signal to Distortion Ration with single tone test)
  - IMD (dB) (Signal to Intermodulation Distortion Ratio with two tone test)
- Local transmitter's nonlinearity can limit the capacity of local receiver , in absence of nonlinear echo cancellation
- Two spec
  - "**Recommended**" spec (compliance not required) :

    essentially a spec on nonlinearity of local transmitter
  - "**Normative**" **spec (compliance required) :**

    ensure that the nonlinearity of a **far end** transmitter does not cause the receiver to lose "much SNR margin"

SFDR & IMD linearity measurement

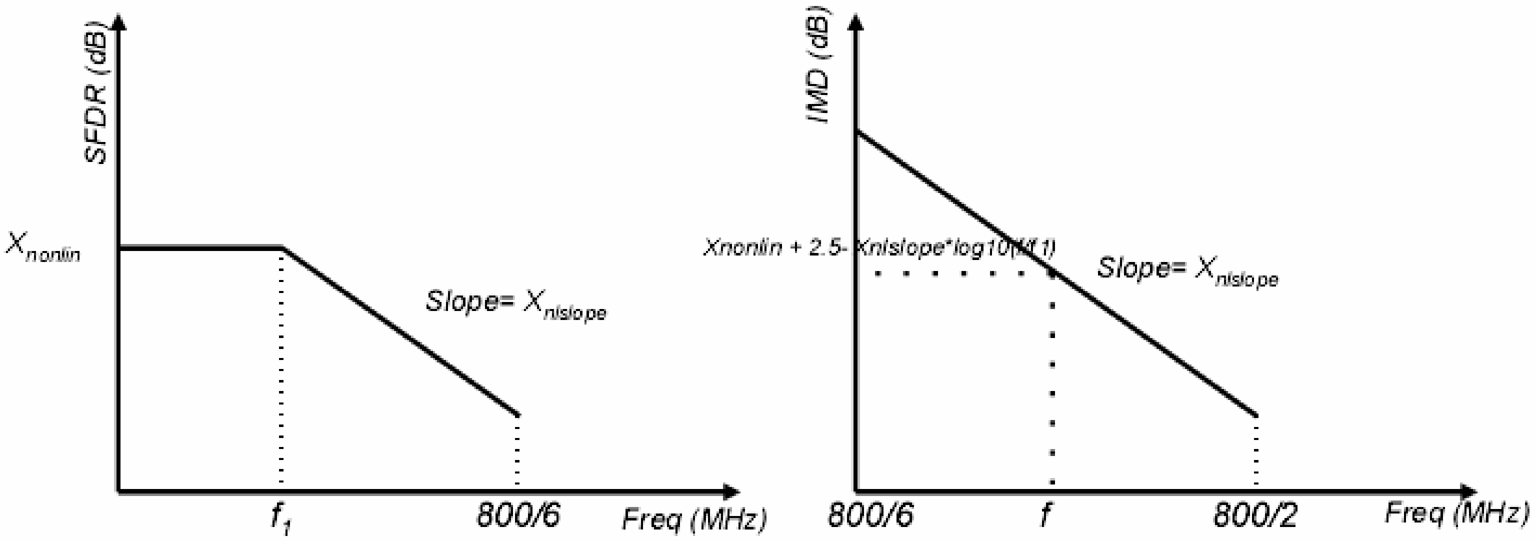
The SFDR of the transmitter when subject to single tone inputs producing output with peak to peak transmit amplitude shall be:

better than X_{nonlin} dB in the frequency range, f ε (0.1, f_1] MHz, f_1 is in MHz

and better than [X_{nonlin}-$X_{nlslope}$*log10(f/f_1)] dB, for f ε (f_1, 800/6] MHz.

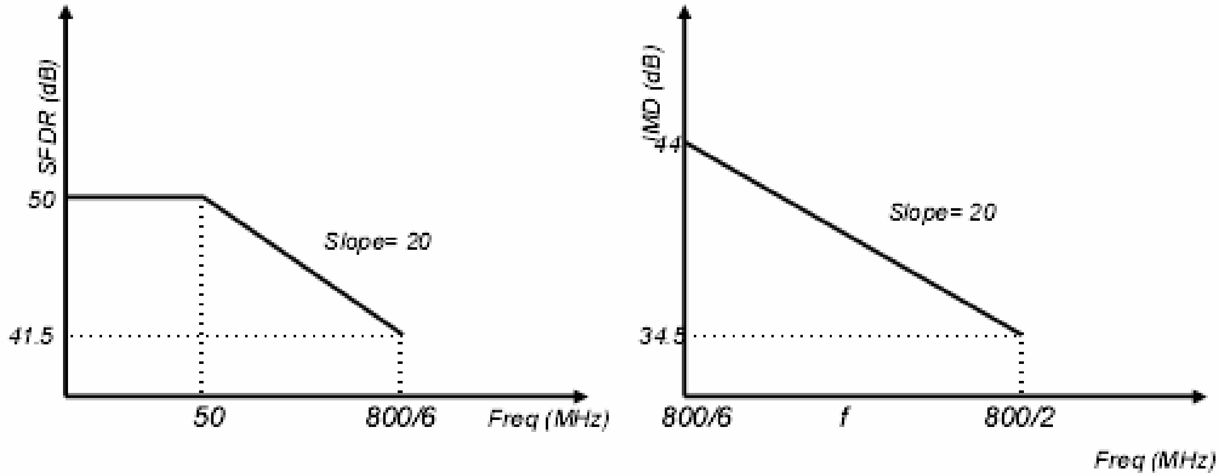
The Signal to Intermodulation distortion ratio of the transmitter, for dual tone inputs, producing output with peak to peak transmit amplitude, shall be better than:

[X_{nonlin} +2.5- $X_{nlslope}$*log10(f/f_1)] dB for f ε (800/6, 800/2]MHz



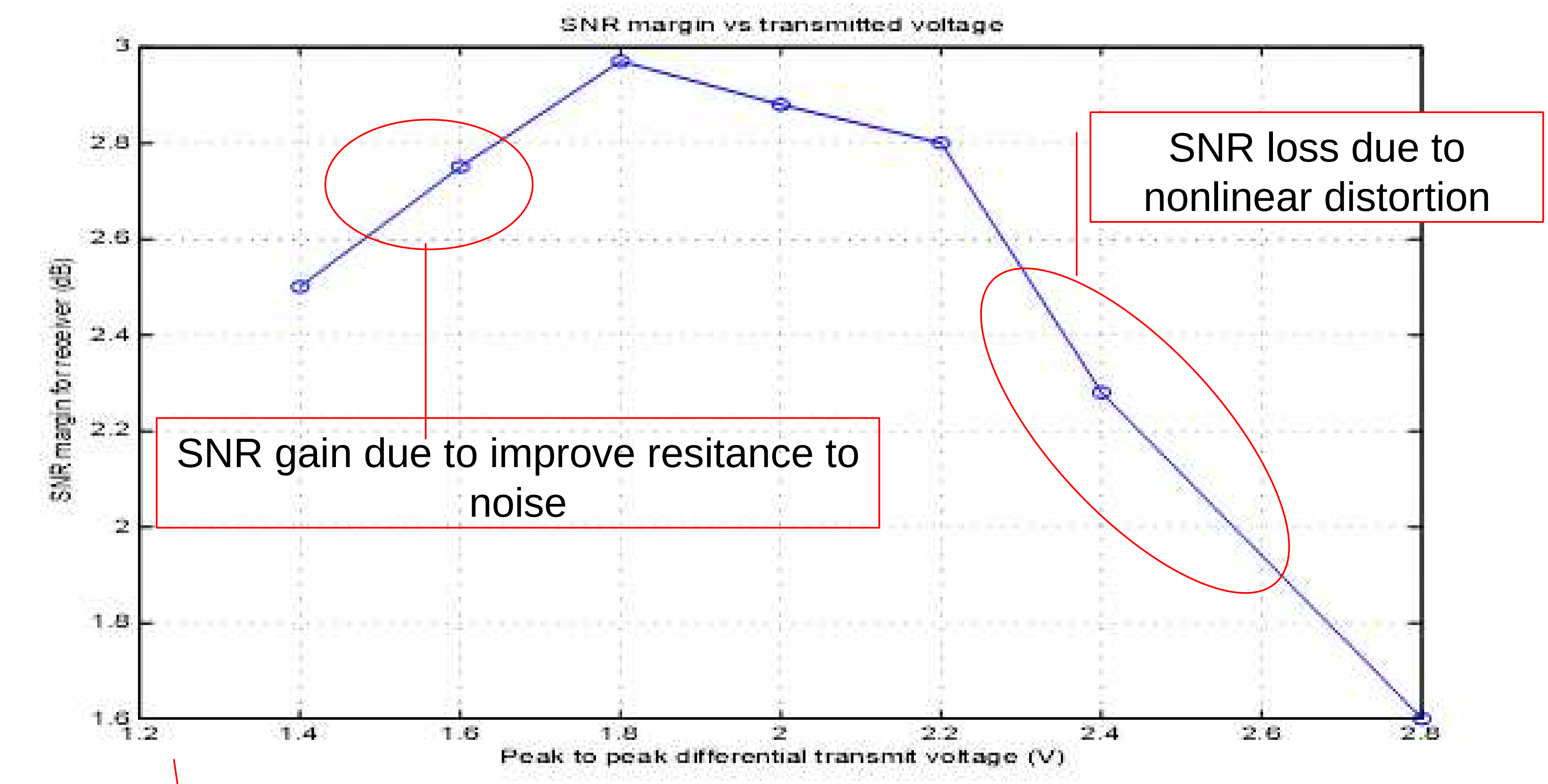
Two linearity spec

- **NORMATIVE SPEC PROPOSAL (compliance required)**: X_{nonlin}=50dB, $X_{nlslope}$=20dB, f_1=50MHz, for equations represented as general in clause 55.4, and repeated in slide 9



- For the "recommended" spec: Similarly, the SNR margin loss due to local transmitter linearity
  - 68dB causes 0.5dB SNR margin loss
  - 65dB causes ~1dB SNR margin loss.
- **RECOMMENDED SPEC PROPOSAL (Compliance not required, just recommended)**: Keep the "recommended" spec X_{nonlin}=65dB, as this is much harder to meet, especially since here $X_{nlslope}$=0, f1=don't care(=400MHz)

TX voltage vs. Receiver SNR margin



Optimal choose transmit voltage (peak to peak) **2V +/- 5 %**
Corresponding to **3.2dbm-5.2dbm** with **4.2dbm** center

TX Bandwidth

- Because of insertion loss , channel gain approaches zero when f > (1/2T) , so excess bandwidth wastes signal energy .

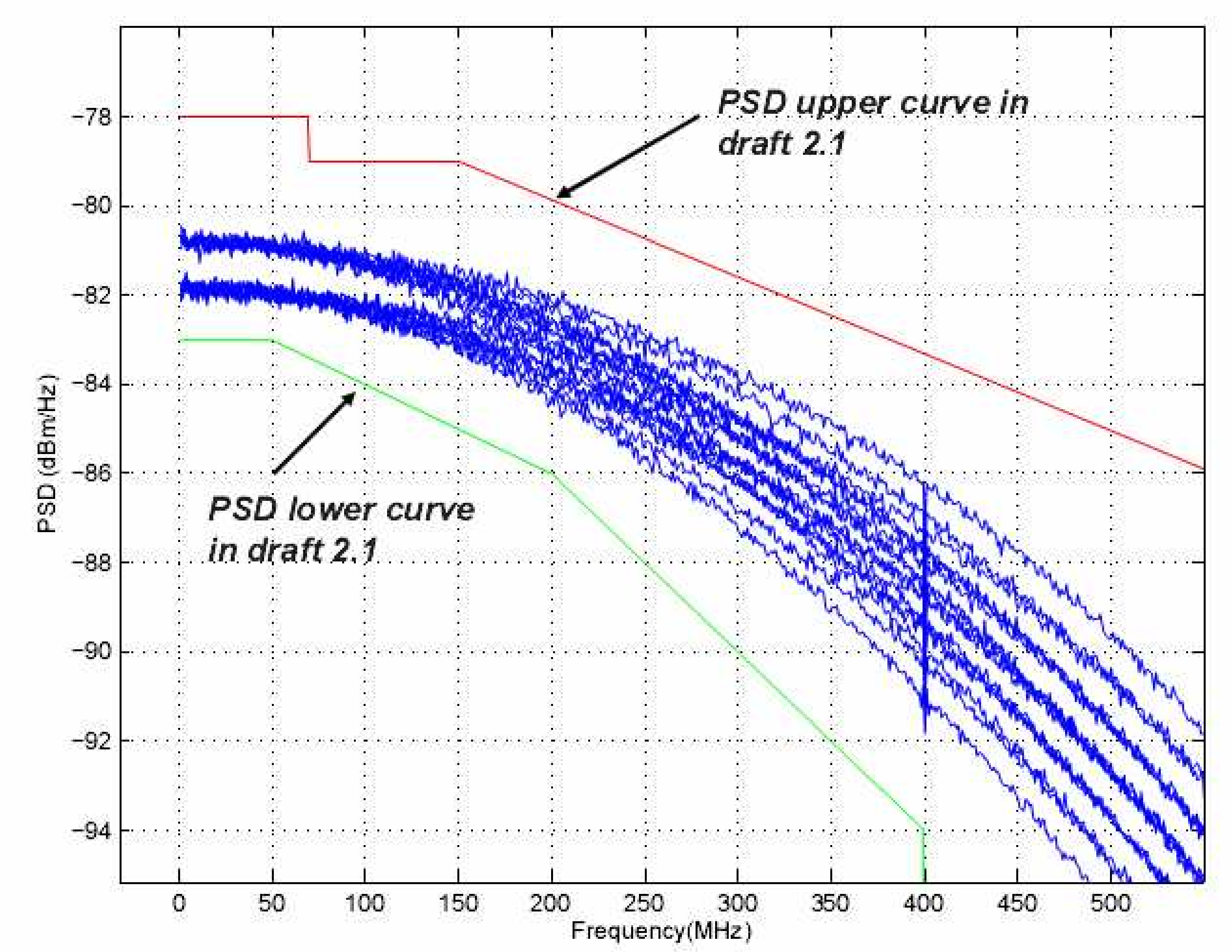
- With zero excess bandwidth , we can use digital interpolation to recover timing with free running clock for ADC .
  ➔Phase insensitive sampling at baud rate

- **Zero excess bandwidth with spectrum null at DC and (1/2T) is desired**

TX PSD(1/3) [Some assumptions for PSD mask]

- PSD mask assumptions
  - Transformer 1st pole at ~100kHz
  - Transformer pole f1 with substantial tolerance of 750MHz +/-33%
  - Transmitter pole f2, "simple filter pole" contributed by the total capacitance at transmitter and 50ohms. This is modeled as 750MHz +/-33% tolerance
  - Transmitter and board "parasitic" pole f3 with substantial tolerance for different implementations, 1200MHz +/- 33%.
  - Sinc roll-off, contributing majority of the band limitation.
- Assume that the voltage on the line side of the transformer, after going in through the transformer Insertion loss (in addition to its bandwidth loss) is 2V +/-6%.
- 2V+/-6% peak to peak differential at the MDI
  - meets the power spec
  - 2V+/-6% spec is better for transmit and echo cancellation linearity. Linearity limits SNR margin.

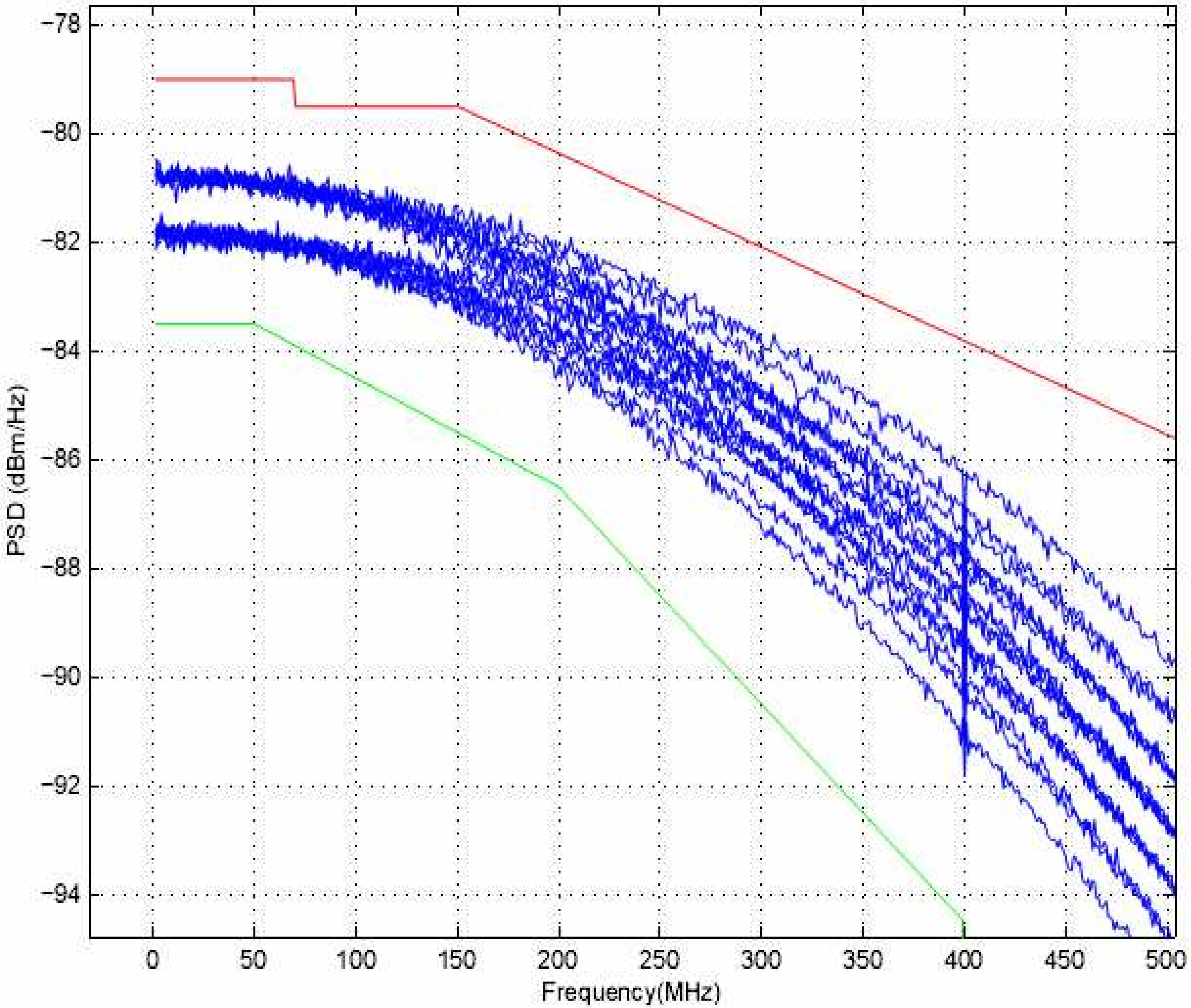
TX PSD (2/3) [PSD in draft 2.1]



Note:

- *With 2V +/- 6% at the transformer output, the lower PSD curve has smaller margin at lower end.*
- *2V +/- 6% with the filter tolerances as specified meets the power spec*
- *Upper PSD has a larger margin, especially the lower 0-70MHz range.*

TX PSD (3/3) [Teranetics' Proposal]



Recommendation:

Reduce the upper PSD by 1dB in 0-70MHz.

0.5dB reduction on upper and lower curves everywhere else w.r.t. draft 2.1, would make it better centered.

PSD upper curve:

-79 dBm/Hz, 0<f<=70
-79.5 dBm/Hz, 70<f<=150
-79.5-(f-150)/58 dBm/Hz, 150<f<=730
-79.5-(f-330)/40 dBm/Hz, 730<f<=1810
-116 dBm/Hz, 1810<f<3000

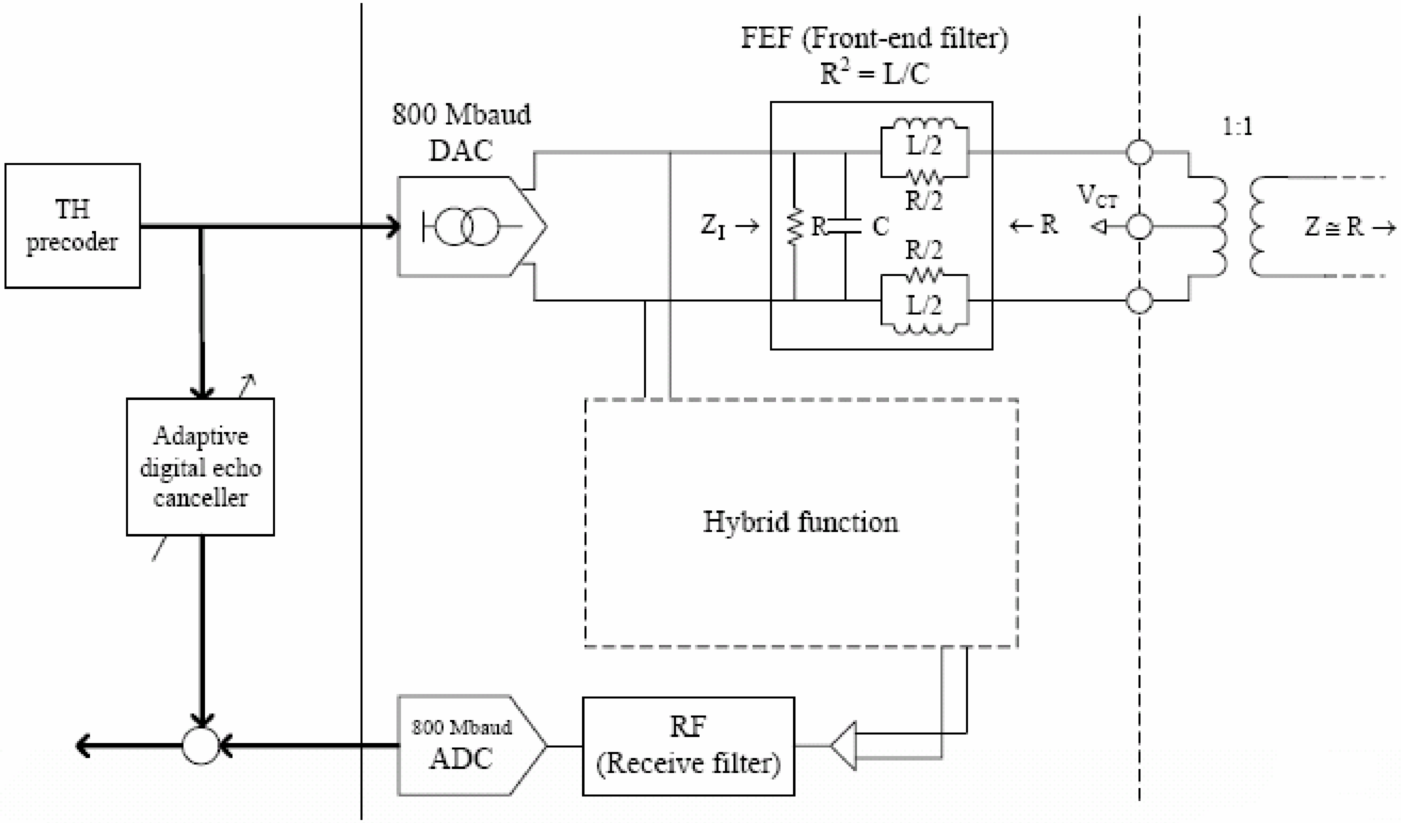
PSD lower curve:

-83.5 dBm/Hz, 5<f<=50
-83.5-(f-50)/50 dBm/Hz, 50<f<=200
-86.5 -(f-200)/25 dBm/Hz, 200<f<=400

Where f and the ranges are in MHz

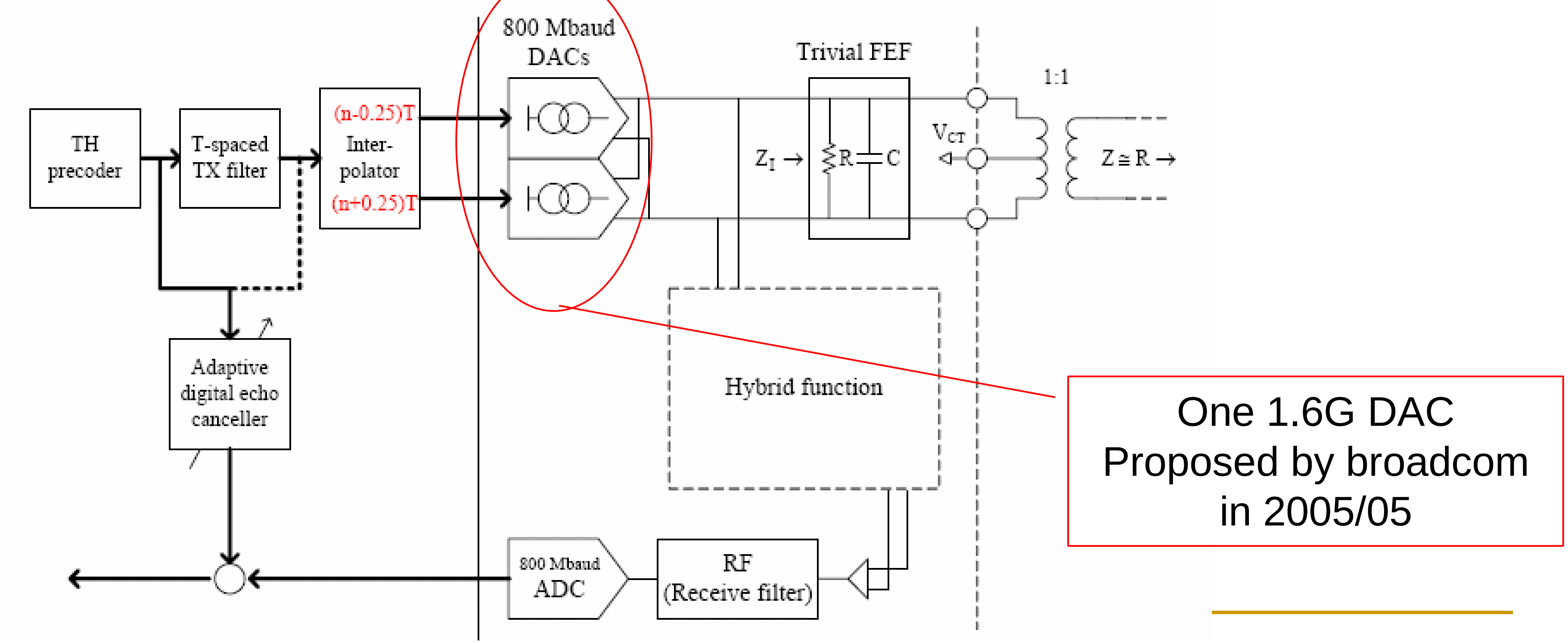
Transmitter front end – only analog TX filter (baseline approach)

- No digital filtering , T-spaced DAC ,TX filter with frequency-dependent input impedance Zi and constant output impedance R



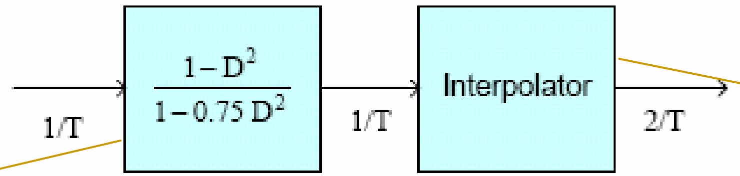
Transmitter front end – Digital TX filter with analog filter (1/3) (oversampled approach)

- Digital TX filtering & T/2-interpolation (Upsampling of 2X) , (T/2) overlapping DAC , trivial front-end analog filter

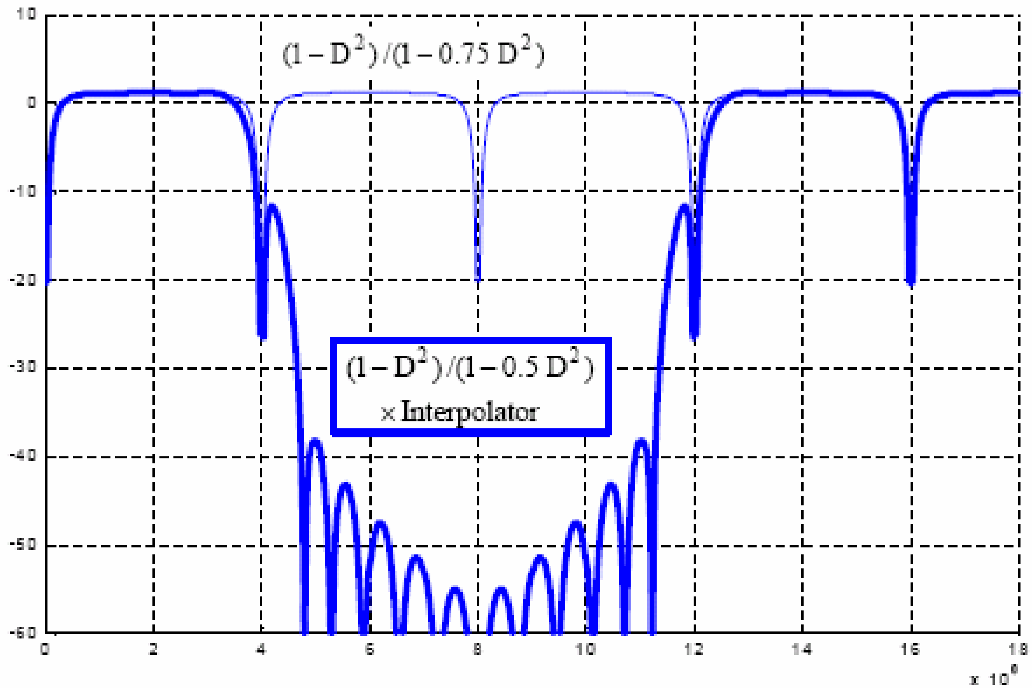


Transmitter front end – Digital TX filter with analog filter (2/3)=>Effect of (T/2) interpolation

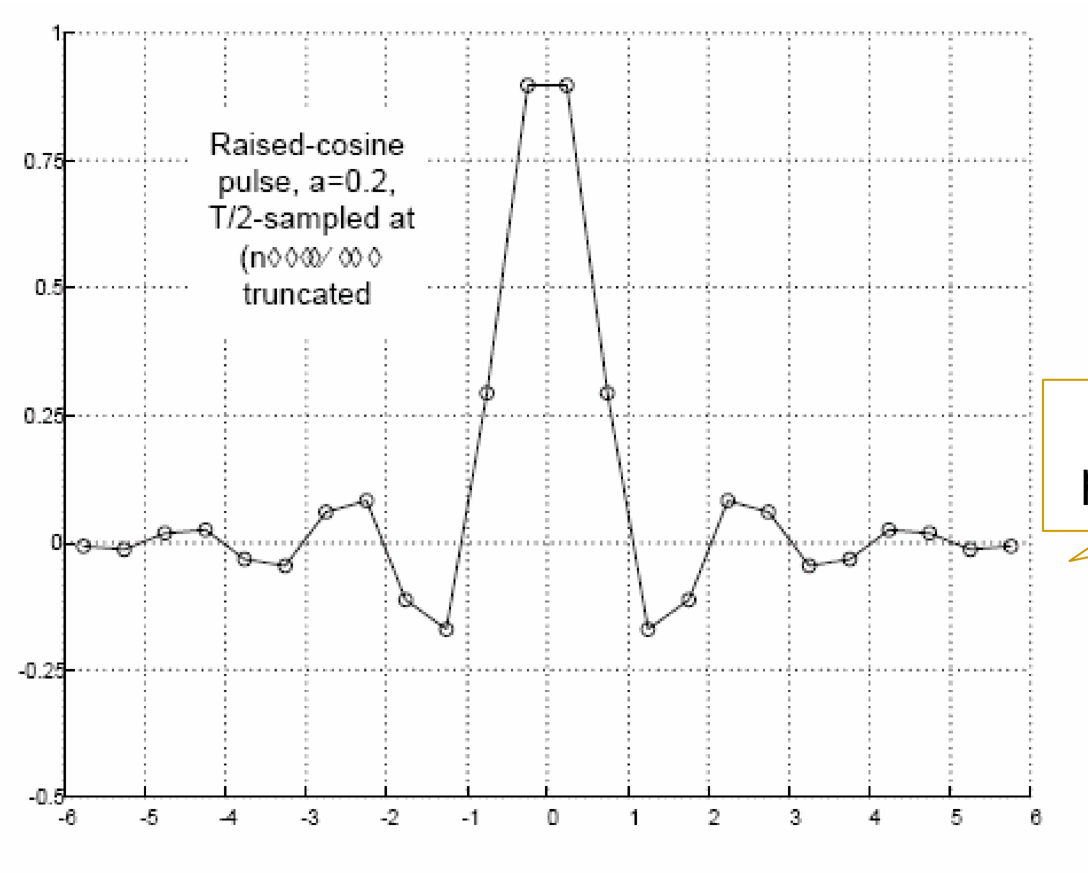
TX filter



Upsampling of 2X
To reduce high frequency component

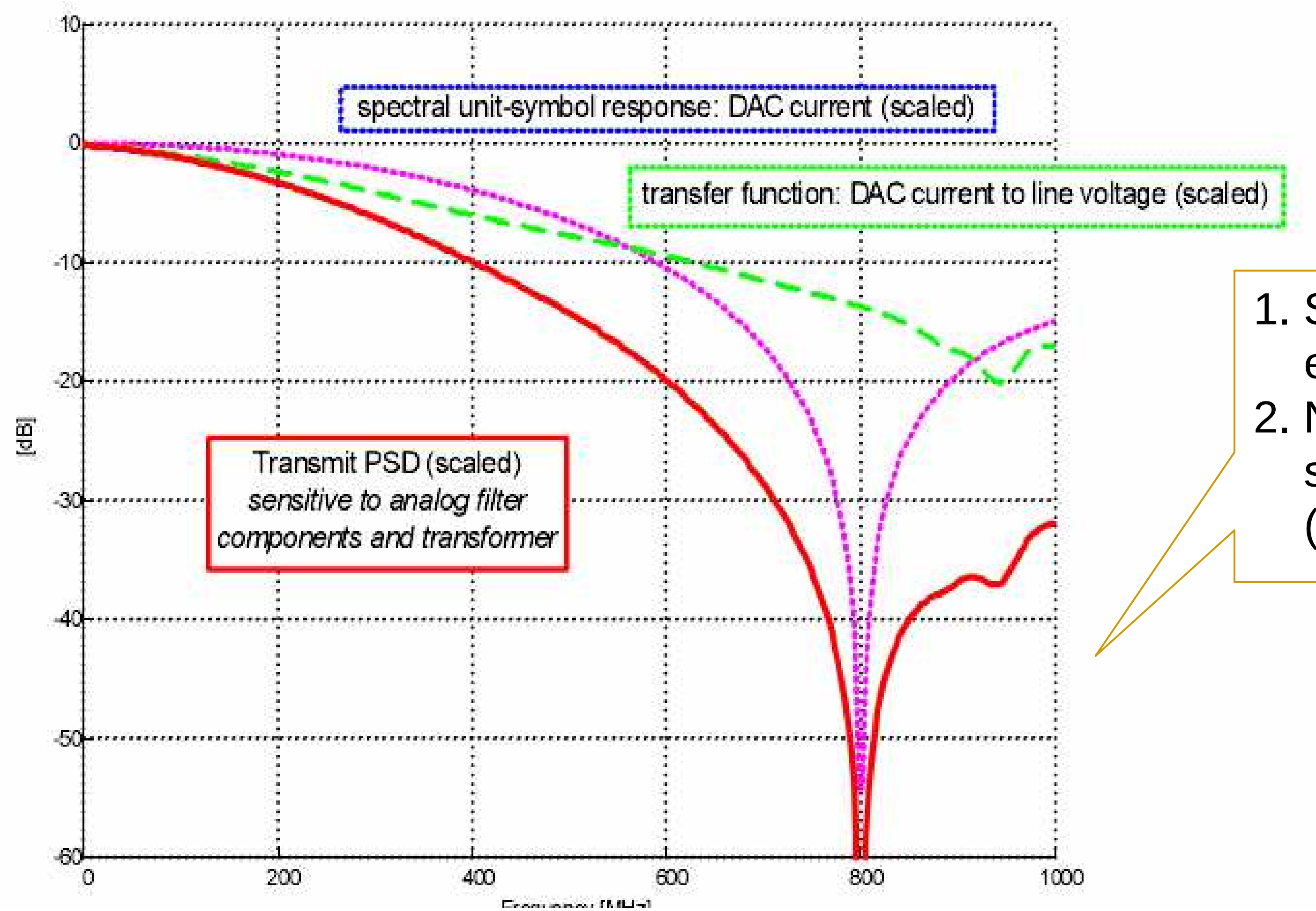


Transmitter front end – Digital TX filter with analog filter (3/3)=>Interpolation coefficients



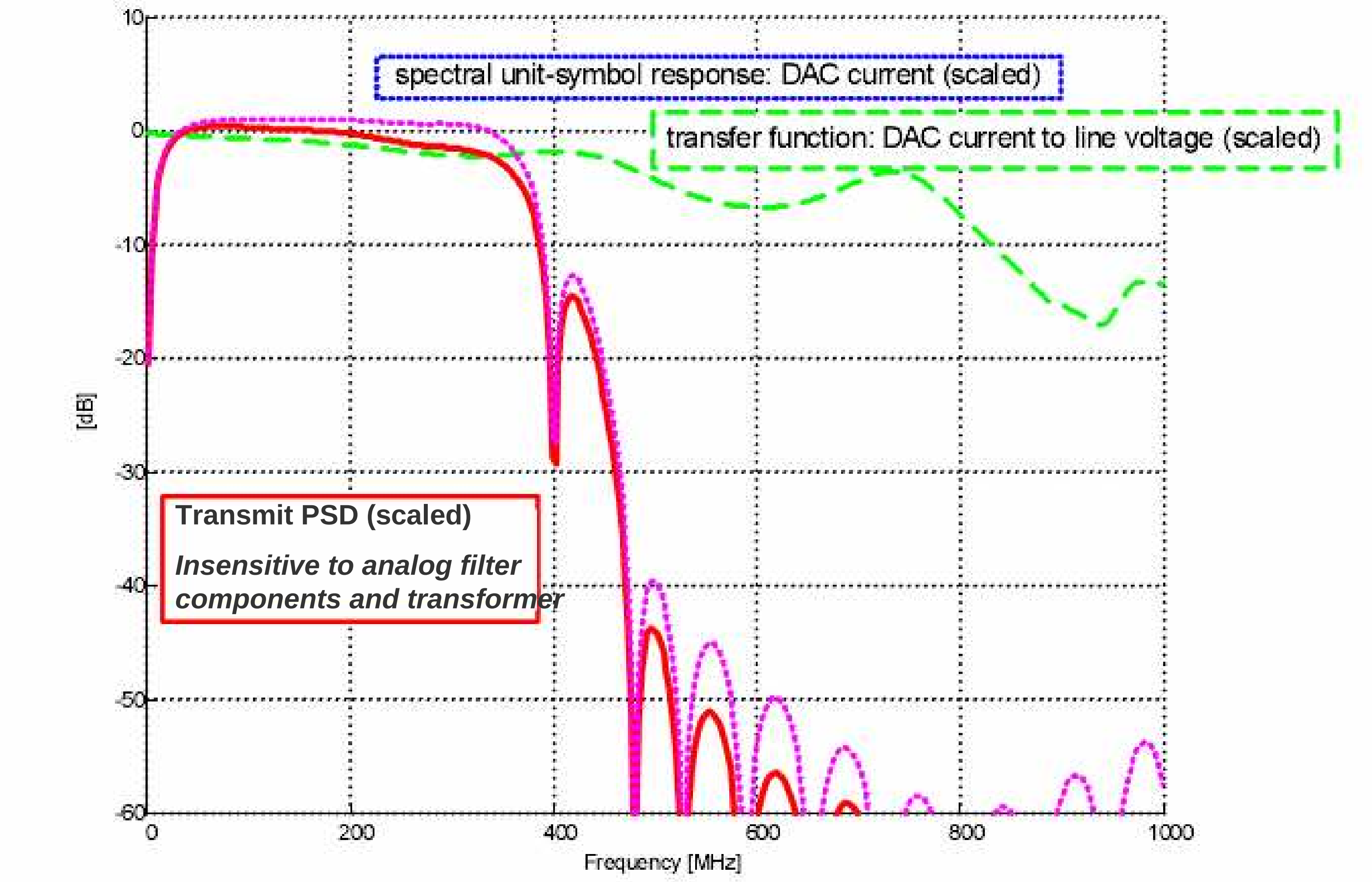
Raised-cosine pulse with a=0.2

Transmitted PSD : Baseline approach



1. Substantial excess bandwidth
2. No controlled spectrum null at (1/2T) and D.C

Transmitted PSD : Oversampled approach



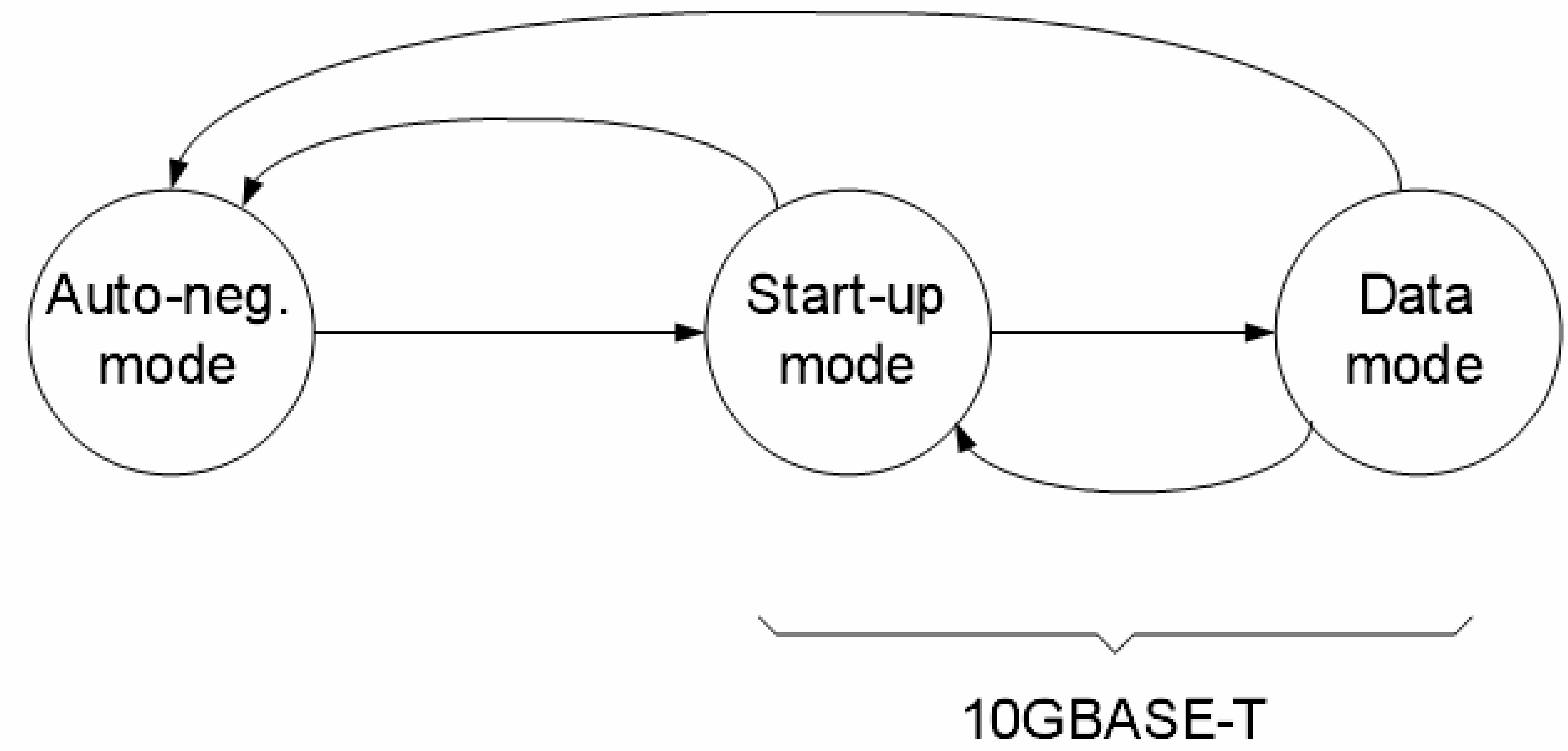
Compare of two approaches

	"Baseline" solution	"Oversampled" solution
Digital filters	none	$(1-D^2)/(1-0.75\ D^2)$ + interpolator
DAC	800 Ms/s	1600 Ms/s
AFE filter	1-st order RLC LPF, f_{3dB}=300 MHz	Trivial R//C
rms and peak voltage at DAC output	higher rms, peak similar to "oversampled"	lower rms, peak similar to "baseline"
Excess bandwidth	substantial (→ sampling phase dependency in receiver)	sharp bandwidth limitation (EMI advantage)
Controlled spectral nulls	none	dc and 1/2T
Return loss	OK	OK
Transmit PSD shape	depends on analog components	digitally defined

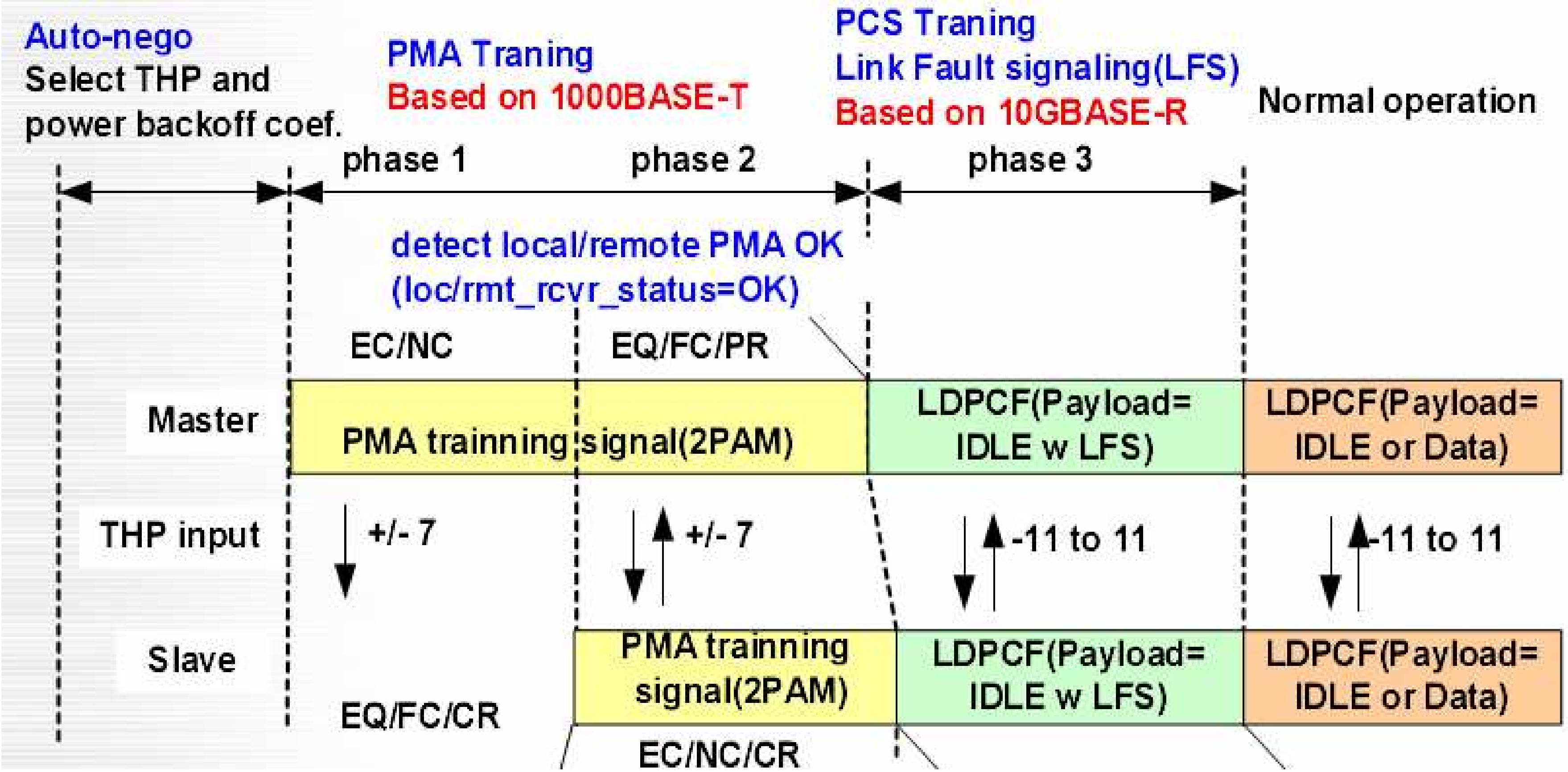
Higher PAR for "oversampled" is compensated by lower rms of "oversampled"

Startup Protocols

Three Operating Modes

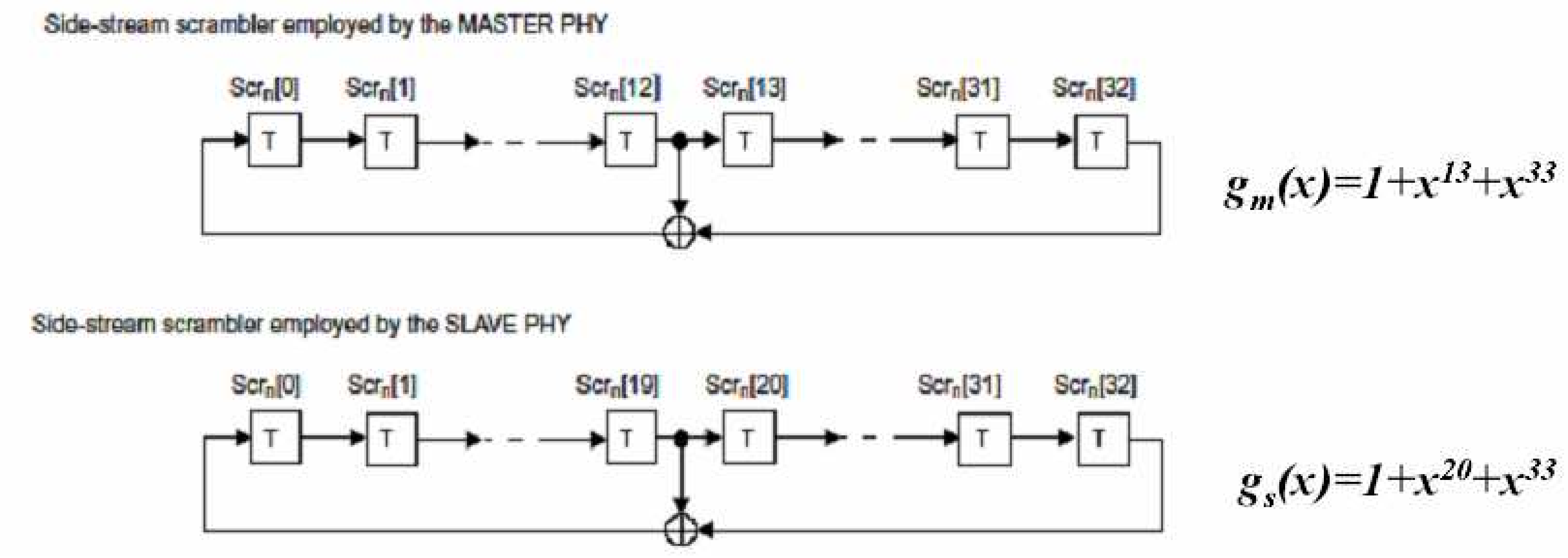


Sequenced Startup

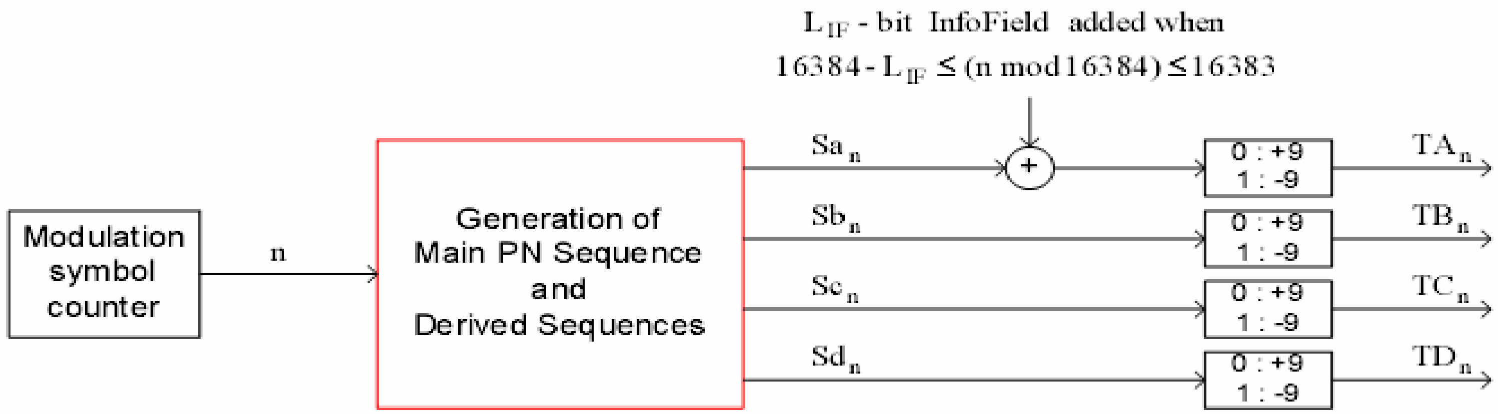


PMA Training Signals(1/2)

- Objective:
  - Recover timing and adaptive filter coefficients
  - Establish polarity correction, pair swap, pair deskew
  - Master and slave use different sequences



Unambiguous generation of PAM training sequences



Main PN sequence

$$n \bmod 16384 = 0: \quad Scr_n[0:32] = 33 \text{ lsbs of } 0x15979A422 \quad \text{(periodic initialization)}$$

$$n \bmod 16384 \neq 0: \quad Scr_n[1:33] = Scr_{n-1}[0:32]$$

$$Scr_n[0] = \begin{cases} Scr_n[20] \oplus Scr_n[33] & \text{if PMA\_CONFIG} = \text{MASTER} \\ Scr_n[13] \oplus Scr_n[33] & \text{if PMA\_CONFIG} = \text{SLAVE} \end{cases}$$

Derived sequences

$$Sa_n = \begin{cases} Scr_n[0] \oplus 1 & \text{if } n \bmod 256 = 0 \\ Scr_n[0] & \text{otherwise} \end{cases}$$

$$Sb_n = Scr_n[3] \oplus Scr_n[8]$$

$$Sc_n = Scr_n[6] \oplus Scr_n[16]$$

$$Sd_n = Scr_n[9] \oplus Scr_n[14] \oplus Scr_n[19] \oplus Scr_n[24]$$

PMA Training Signals(2/2)

- There is only one pair combination which satisfy all equations become 0

Polarity correction

$$Ry_n[x] \wedge Ry_{n-13}[x] \wedge Ry_{n-33}[x] = \begin{cases} 0 \text{ (polarity = OK)} \\ 1 \text{ (polarity = NG)} \end{cases} (x = 0,1,2,3)$$

$Ry_n[x]$: PAM2 demapping data of Lane x

Pair swap, deskew

$$Ry_n[x] \wedge Ry_{n-3}[x-1] \wedge Ry_{n-8}[x-1] = \begin{cases} 0 \text{ (skew = OK)} \\ 0/1 \text{ (skew = NG)} \end{cases} (x = 1,2)$$

if (remote side PMA status = NG)

$$Ry_n[3] \wedge Ry_{n-3}[2] \wedge Ry_{n-8}[2] \wedge Ry_n[0] = \begin{cases} 0 \text{ (skew = OK)} \\ 0/1 \text{ (skew = NG)} \end{cases}$$

else

$$Ry_n[3] \wedge Ry_{n-3}[2] \wedge Ry_{n-8}[2] \wedge Ry_n[1] = \begin{cases} 0 \text{ (skew = OK)} \\ 0/1 \text{ (skew = NG)} \end{cases}$$

References

[1] M. Hatamian et al. , "Design considerations for gigabit Ethernet 1000Base-T twisted pair transceivers , " Proc 1998 IEEE Custom Integrated Circuits Conf . ,pp. 335-342 , May 1998.

[2] Kamran Azadet , "Gigabit Ethernet over Unshielded Twisted Pair Cables ," in Proc. Int. Symp . VLSI Technology , Systems , and Applications , Taipei , Taiwan , Jun. 1999 , pp. 167-170 .

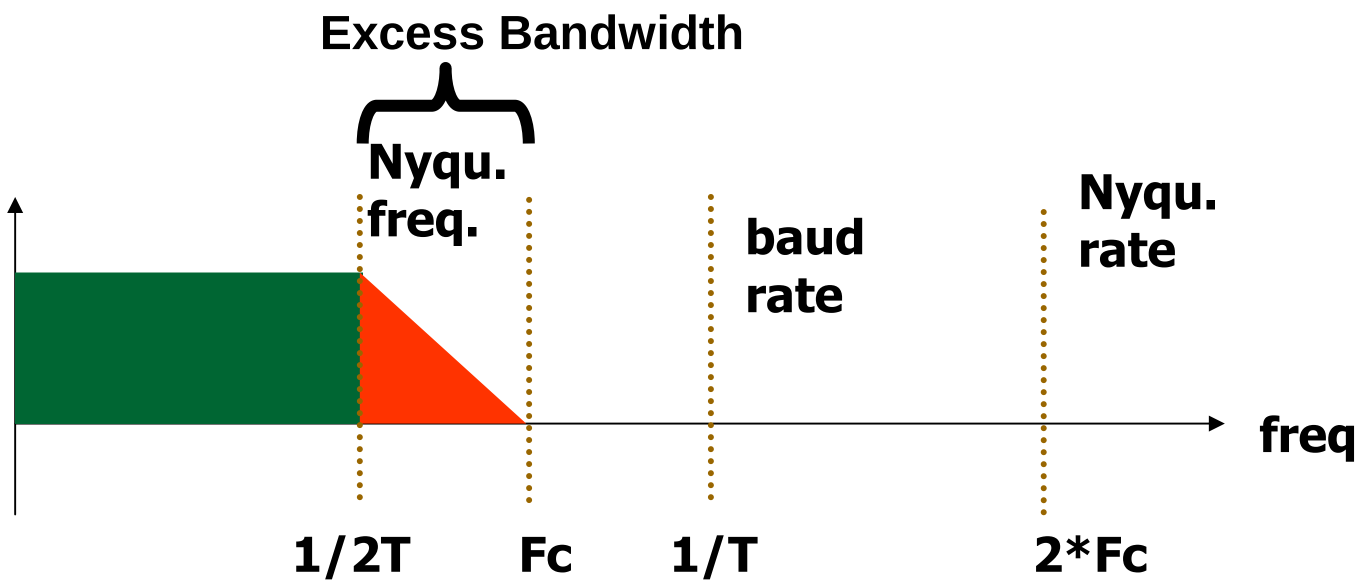
[3] Jingyu Huang and Richard R. Spencer " The Design of Analog Front Ends for 1000BASE-T Receivers " IEEE TRANSCATIONS ON CIRCUITS AND SYSTEMS –II : ANALOG AND DIGITAL SIGNAL PROCESSING , VOL. 50 ,NO. 10 , OCTOBER 2003

[4] http://www.ieee802.org/3/an/ (Mainly from Vendor : Broadcom)

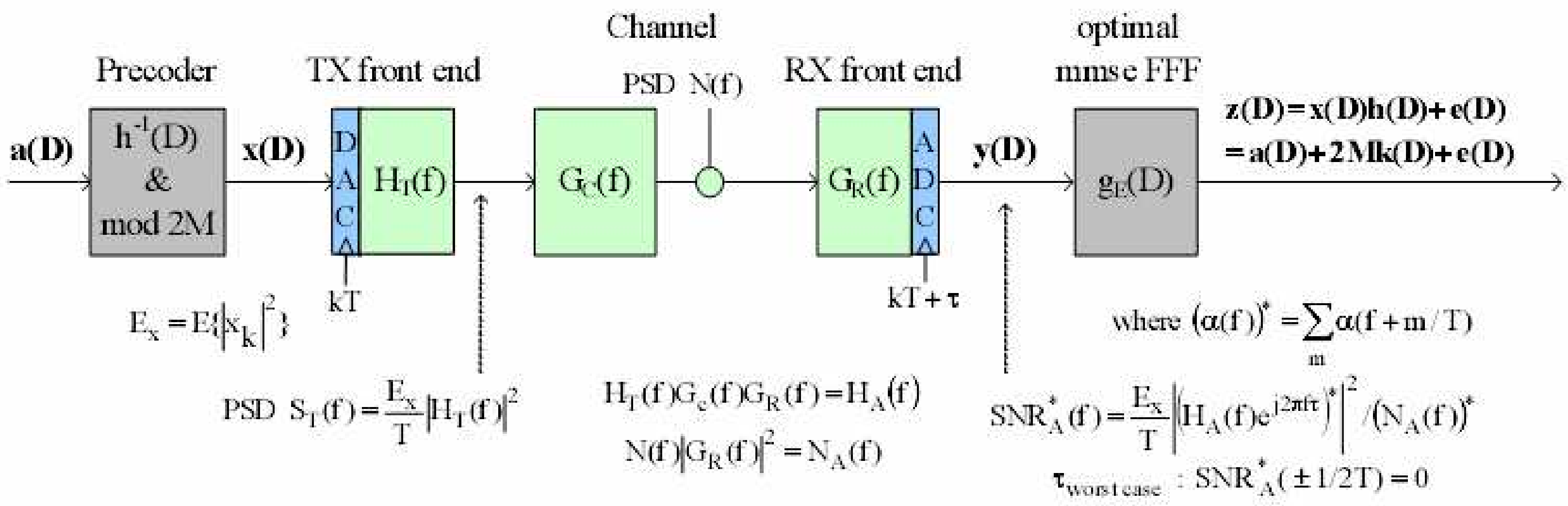
Back slides

Concept of excess bandwidth

- From sampling theorem, no info. is lost with baud-rate sampling
- all sampling phase convey the same amount of timing information (interpolator)



THP coefficients calculate



Decision - point SNR for given $H_A(f)$, $N_A(f)$, τ, and precoding response $h(D)$

$$SNR_{mmse}=\left[T\int_{-1/2T}^{1/2T}\left|h(D=e^{-j2\pi fT})\right|^2/\left(SNR_A^*(f)+1\right)df\right]^{-1},\quad h(D)=1+\sum_{\ell=0}^{L}h_\ell D^\ell$$

For given $SNR_A^*(f)+1$, determine (arg) $\max\limits_{h_1,h_2,\cdots h_L} SNR_{mmse}$.